Chapter 1
Radiation Effects in CMOS Technology

1.1 Radiation and Its Interaction with Matter

This chapter will introduce the radiation effects that are encountered in modern CMOS technologies that have been used in this work. A summary of the effects and the potential problems will be discussed.

To understand the damaging effects of radiation on silicon devices, a brief introduction on particle interactions is required. Radiation consists of sub-atomic particles or photons which may interact with matter as they travel through space. Significant research has been done, and is still being done, on how these particles interact with matter but the main mechanism will be listed briefly in this chapter. For CMOS technologies, the interaction of radiation with Si and SiO_2 is of main interest since the majority of the damage is observed in these materials of the devices.

Radiation can be sub-divided into two major categories, ionizing and non-ionizing radiation [1]. Ionizing radiation directly leads to ionization of the atoms of the matter which it passes through. This means that electrons are separated (temporarily) from the atom leading to free electrons and ionized atoms. Charged particles (like electrons, protons, ions, etc.) and photons can be involved in an ionization process. Non-ionizing radiation does not directly ionize the atoms and thus does not generate free charges as it passes through matter. Non-ionizing radiation are neutral particles (like neutrons and neutrinos) which have no charge and thus do not interact with the atoms' electrons. Neutrons do interact with matter through nuclear reactions between the neutron and the nuclei of the atoms. Reactions like "neutron capture" convert the matter's nuclei to different isotopes which may be unstable and decay to two lighter elements.

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1.1.1 Direct Ionization

Ionizing radiation, excluding photons, can ionize atoms through coulomb forces between charged particles and the electrons of the target material [2]. Electric forces acting on the electrons may be strong enough to separate them from the atom. These electrons can become "free" electrons when the energy transferred to the electron is larger than the ionization energy of the atom. For silicon, this energy is 3.6 eV and is the energy required to bring an electron from the valence band in the conduction band.

Figure 1.1 shows an example of an ionization of an electron in a silicon bandgap. The bandgap of silicon is 1.1 eV but since silicon is a non-direct semiconductor, the ionization happens through a phonon generation in the lattice. To allow this, an energy of 3.6 eV is required which is partially transferred to the electron and phonon to ensure a conservation of energy and momentum.

Coulomb forces between charged particles and the atoms' electrons can happen as is shown in Fig. 1.2. These effects are called direct ionization. A charged particle can pull or push to the electron when being in its neighborhood. With sufficient force, the electron can be separated from the atom leading to an ionized atom. Positive particles can cause direct coulomb collisions with the electrons pushing them out of the atom's orbitals. If charged particles like electrons and positrons travel in a potential field, the electric forces will bend the trajectory of the particle leading to additionally generated photons, more known as "bremsstrahlung" which may result in secondary ionization effects.

Heavy ions ionize in a similar way but can also cause collisions with the nuclei giving nuclear reactions resulting in lighter ionizing particles which again lead to ionization.

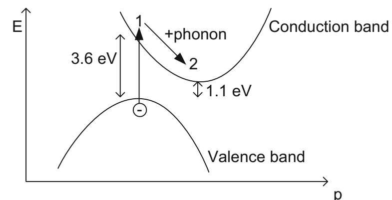


Fig. 1.1 Electron ionization in indirect bandgap semiconductors requiring more energy than the bandgap energy. The graph shows the energy bands as a function of the electron momentum

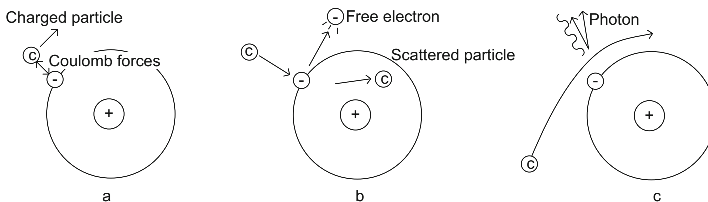


Fig. 1.2 (**a**) Coulomb force interaction (**b**) Coulomb collision (**c**) Bremsstrahlung

1.1.2 Electromagnetic Radiation

Photons are a special case of ionizing radiation [3]. X-rays and γ rays consist of highly energetic photons. Since photons have no charge and mass, they cannot interact with matter in the ways discussed previously. There exist no coulomb forces between the photon and the electrons. Photons interact with matter through the photoelectric effect, Compton scattering, or pair production as is shown in Fig. 1.3 [4]. Even though the mechanisms are different compared to coulomb forces, the result is the same, free electrons. Einstein's theory posed that free electrons are observed when a cathode is irradiated with photonic-radiation. The energy and momentum of the photon is absorbed by the electron and the atom and the excess energy above the ionization energy is converted into kinetic energy of the electron. Compton scattering is similar to the photoelectric effect in which the photon is not completely absorbed. The photon interacts with the target electron transferring part of its energy and momentum to the electron, again leading to free electrons when the energy is sufficient. Finally, free electrons can be generated when no electrons exist. This effect is called pair production in which an electron and a positron are generated from a photon. This requires a minimum energy for the interaction to occur since the rest mass of both particles requires a minimal energy to be created ($E = m_{rest}c^2$, where m_{rest} is the combined rest mass of the electron and the positron). The minimum energy for this event is 1.02 MeV. Additionally, the excess energy transferred to the electron should be sufficient to be a free electron. This reaction only occurs when the photon is at an interaction point, like nucleon and does not happen in free space since it requires a conservation of momentum.

In Fig. 1.4, the probability is shown for these three effects to occur. The photoelectric effect occurs at low photon energies. The probability reduces when the photon energy is higher since the momentum of the photon has to be transferred to the electron. At moderate energies, Compton scattering is therefore more likely. For higher energies, the photons are absorbed through pair production which dominates Compton scattering [4].

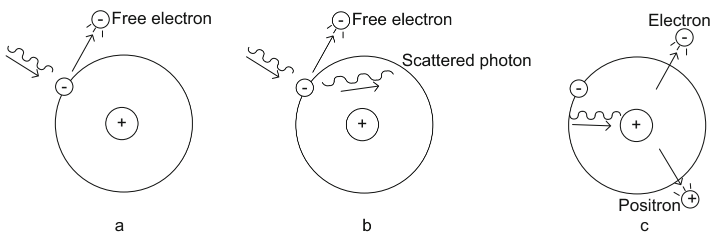


Fig. 1.3 (**a**) Photoelectric effect (**b**) Compton scattering (**c**) Pair production

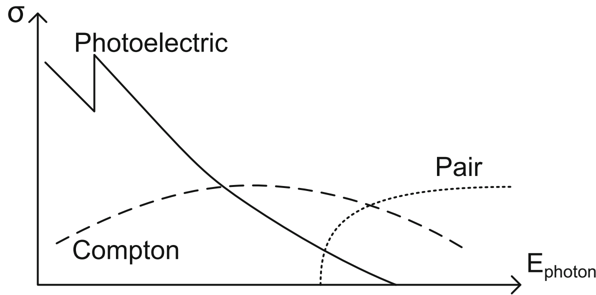


Fig. 1.4 Cross sections (probability) of the photon interactions as a function of photon energy

1.1.3 Neutrons

When neutrons travel through matter, they may interact with the nuclei of the atoms and not directly with the electrons. When a neutron is in the range of the target nuclei, it can be captured by the nuclei [5]. This effect is called neutron capture. Since neutrons are not charged, they are not repelled by the atom. An additional neutron can make the nuclei unstable and decays to smaller fragments. The target nuclei typically decay to smaller elements with an additional α-particle and photon. These secondary particles, generated from the nuclear reaction can lead to ionization referred to as indirect ionization since the neutrons do not directly ionize the atoms. Since the neutron has to directly interact with the nucleus and has to destabilize the nucleus, it takes some time for the reaction to occur. This is the reason why slow (low energy neutrons) have higher cross section (the spatial probability for an interaction to occur) compared to fast (high energy) neutrons since the potential interaction time of slow neutrons is higher than fast neutrons. A big portion of the energy is not converted into free electrons. This energy is called Non Ionizing Energy Loss (NIEL).

1.1.4 Effects on Semiconductors

The above discussion briefly introduces the basic interactions of charged particles, photons and neutrons with matter leading to ionized atoms and free electrons. To discuss radiation effects in CMOS devices, generated electrons are important. Note that, when a free electron is generated from a stable atom within a semiconductor, a hole is also generated in the ionized atom. Therefore, it can be said that nuclear radiation generates electron-hole pairs in the semiconductor such as silicon. The same holds true for SiO2 with the difference of a larger band gap.

The generation of electron-hole pairs is the first step in the radiation damage in semiconductors. In the second step, these charges change the electric characteristics of the devices. These effects are discussed in Sect. 1.2. Furthermore, these free electrons lead to transient currents after they are generated inside the transistors of the circuits. These effects and mechanisms are discussed in Sect. 1.3. Radiation effects require additional simulations to predict the behavior of the circuit after or during irradiation. This has become difficult in modern technologies. A simulation flow is introduced in Sect. 1.4.

1.2 Total Ionizing Dose Effects

Total Ionizing Dose (TID) effects on CMOS technologies originate from trapped charges in the oxides around the transistors. When ionizing radiation passes through the transistors' oxides, SiO_2 atoms are ionized and electron-hole pairs are generated. In the old technology nodes, from 0.13 μm and above, the majority of the radiation effects were seen in the gate oxide where charges were trapped. While many circuits resort to technologies with smaller feature size, the basic charge trapping mechanisms remain valid in deep submicron CMOS technologies.

1.2.1 Basic Charge Trapping in CMOS Transistors

The basic charge trapping mechanism is shown in Fig. 1.5 which shows the energy band of the gate, oxide, and silicon interface [6]. The charge trapping happens in three phases. In the first phase, when an ionizing particle crosses the oxide, electron-hole pairs are generated inside the oxide. As discussed before, one particle may generate multiple pairs depending on its total energy and interaction with the oxide. After the atoms are ionized, a fraction of these free electrons will immediately recombine without creating any damaging effects in the transistors. The remaining free electrons which do not recombine are relatively mobile in the oxide and are collected by the gate node under positive bias (nmos). This results in positively charged holes left in the oxide. In the second phase, these positive charges migrate in the oxide through localized states towards the silicon interface [6]. The hopping mechanism has been known to be thermally and electric field activated. Once they finally arrive near the silicon interface, the charges can be trapped and remain present in the device.

Since the trapped charges are positive [7, 8], they change the threshold voltage due to oxide traps (V_{ot}) of the devices by

$$V_{ot} = -Q_{ot}/C_{ox} \tag{1.1}$$

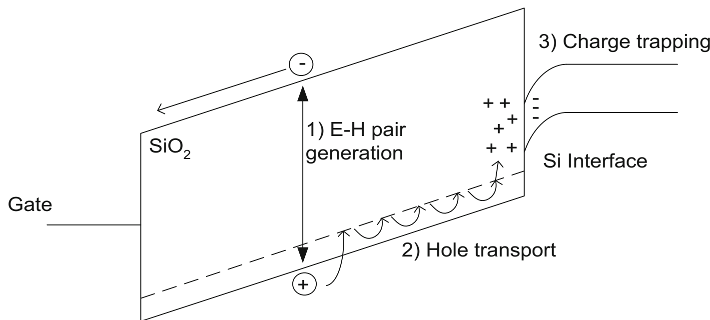


Fig. 1.5 Band energy representation of the gate-oxide-silicon interface and the mechanism of positive charge migration and trapping

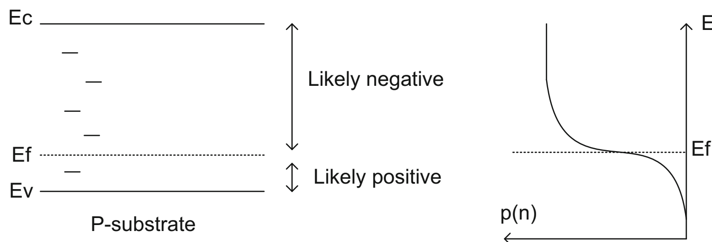


Fig. 1.6 Bandgap of a P-type substrate and probability of charges in the traps within the bandgap. E_f, E_c, and E_v are the fermi, conduction band, and valence band energy, respectively

The amount of charge which is generated by the radiation is directly proportional to the gate thickness since a thicker oxide has more yield in generating charges. Therefore, the threshold voltage shift is directly proportional to t_{ox}^2.

$$V_{ot} \propto t_{ox}^2 \tag{1.2}$$

From this result it can be concluded that scaled technologies are advantageous for TID effects since thinner gates capture fewer charges and have higher C_{ox} [9].

Besides, charges generated in the oxide, the radiation damage leads to a buildup of traps near the interface of the SiO_2 [10, 11]. These traps can be neutral, donor or acceptor type. In nmos transistors, which are fabricated on a p-substrate, the fermi potential is below the midband energy. Therefore, energy levels within the bandgap are likely to be trapped by negative charges. For pmos devices, these traps are occupied by positive charges since the fermi potential is above the midband energy level. Figure 1.6 shows an energy band diagram of a P-type substrate (nmos transistor) with the probability of a negative charge at a given energy level. These probabilities follow the Boltzmann distributions of excess carriers in the semiconductor [12].

While oxide trapped charges are positive for both nmos and pmos transistors, trapped charges due to radiation induced traps are positive for pmos devices but negative for pmos devices [13].

The overall threshold shift can be calculated as the sum of oxide traps (Q_{ot}) and interface traps (Q_{it}) for P− and nmos devices

$$V_{tot} = V_{ot} + V_{it} = -\frac{Q_{ot} + Q_{it}}{C_{ox}} \quad (1.3)$$

For pmos transistors, both Q_{ot} and Q_{it} are positive such that both effects lead to a negative shift of the threshold voltage. In nmos devices, oxide traps are positive while interface traps are negative leading to a competing effect. Since interface traps are observed at a later stage after irradiation, typically a reduction of the threshold voltage is observed in the first phase while later, the threshold voltage increases again.

The above results discussed suggest that TID effects are uniform on all devices on the chip. This is true if the irradiation gradient is zero (which can be assumed for small chips) and the devices are identical. The latter is not the case since local process variations make each transistor unique. In [14], experiments were done on the mismatch between CMOS transistors before and after irradiation from which it has been found that the variability increases with the dose which is likely due to the impact of random dopant fluctuations on TID effects.

Finally, leakage currents increase as well in nmos transistors due to the reduction of the threshold voltage. This can become a dramatic concern in large digital chips since the power grid may become insufficient [15].

1.2.2 Narrow Channel Transistors

The mechanisms described above are originating in the gate oxide and were the major contributions in old technologies. However, as transistors shrunk in both length and width, secondary effects started to occur in other relevant oxides in the transistor [16]. A narrow transistor is a transistor which has relatively large length but small width.

Figure 1.7 shows the layout of a narrow nmos transistor and its cross section. To define the width of the channel, STI (Shallow Trench Isolation) is used which is SiO_2 oxide. As the gate oxide can trap positive charges, so do STI oxides. The STI however is significantly wider compared to the gate oxide and can trap much more charges than the gate oxide. However, its effect is only seen near the edges of the transistor [17]. Therefore, the STI oxide traps become significant when the width of the transistor is shrunk such that the edge effects of the trapped charges become relevant and change the behavior [18]. Wider devices are less influenced by the STI traps since the channel potential disturbance only happens near the edges.

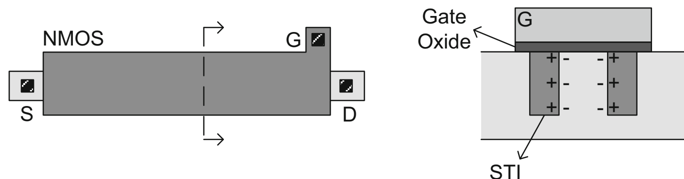


Fig. 1.7 Narrow nmos transistor and its cross section. Positive trapped charges disturb the local potential in the channel near the edges of the transistor

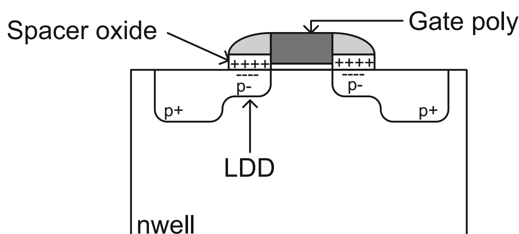


Fig. 1.8 Positive oxide traps below the LDD spacers invert the p− implants which leads to an increased series resistance

1.2.3 Short Channel Transistors

In a short channel device, for which the length is small, a different and significant important effect is observed from TID measurements which is disastrous for pmos devices. Figure 1.8 shows a cross section of a short pmos transistor. To reduce the electric fields in the channel, LDD (Local Drain Diffusion) is used in modern devices. This reduces hot carrier injection to improve the reliability of the devices. The LDDs are fabricated through spacers at the edges of the poly gates which prevent highly doped source-drain implants below the spacers. These spacers are associated with a relatively thin (15 nm) oxide. For pmos devices, this results in locally low-doped p− extends of the highly doped p+ source and drain.

Similarly to the gate oxide and STIs, this oxide below the spacer can also trap positive charges. As a result, the local effective doping of the p− LDD is further reduced since the positive charges in the oxides below the spacers influence the potential in the LDD. This leads to a tremendous increase of the resistance of the LDD spacers [16].

The effect is happening for all different lengths of the pmos devices but becomes visible as the length becomes shorter and the ratio between the LDD resistance and the channel conductivity becomes larger.

This effect is seen in pmos devices since the implants are positive. For nmos transistors, the n− LDD implants become stronger. It is believed that this reduces the effectiveness of the LDD and increases the hot carrier injection [19, 20]. Measurement results have also shown that the degradation is highly asymmetrical showing that the main degradation is happening near the drain of the nmos devices as a result of increasing hot carriers [16, 21].

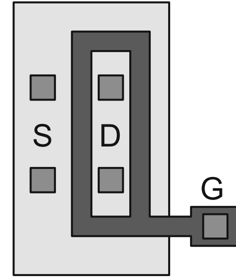


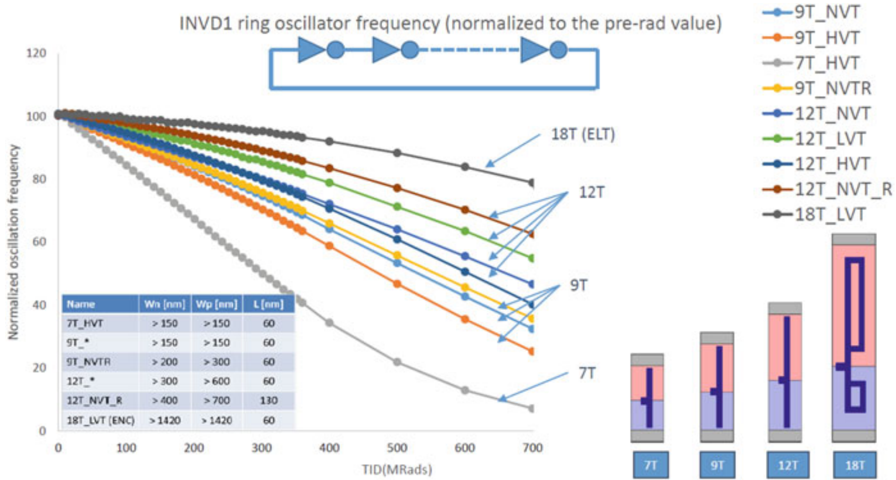
Fig. 1.9 Enclosed layout transistor to mitigate edge effects in narrow transistors

1.2.4 Enclosed Layout Transistors

The effect of STI can be eliminated by the use of Enclosed Layout Transistors (ELTs) [22]. In an ELT, as is shown in Fig. 1.9, the drain or source is fully enclosed by a gate which excludes any edges in the transistor and avoids the effect of those charges. To meet the design rules of the technology, the minimum width of an ELT is typically much larger compared to a minimum sized linear transistor which leads to a significant increase of the power consumption in digital circuits which employ standard cell libraries that are designed with ELTs [23]. However, as the sizes of the transistors increase, the radiation hardness is significantly improved. An experiment was performed in [24] to investigate the degradation of the speed of digital cells. Since the speed is proportional to the drive current, the cells become slower with increasing dose. Figure 1.10 [24] shows the speed reduction for different standard cell libraries in the same technology. It can be seen that small cells (7 track) are significantly more sensitive to TID compared to larger cells. Clearly the ELT outperforms all libraries since it eliminates the edge effects in the transistors. However, the 18 track ELT library contains the smallest transistors that could be used to comply with the foundry DRC rules.

1.2.5 Experimental Results

Experiments were performed in [16] to investigate the radiation hardness of a 65 nm CMOS process. During these experiments, devices with different geometries were measured. Figure 1.11 [16] shows the current through a pmos device which shows the effect of narrow and short devices. Narrow transistors degrade through STI trapped charges while short transistors degrade through LDD resistance. Therefore, the combination of short and narrow devices is the worst. It is clear that the ELTs perform best in the experiment since no STI effects occur. The remaining degradation originates in the LDD short channel effects.



Name	Wn [nm]	Wp [nm]	L [nm]
7T_HVT	> 150	> 150	60
9T_*	> 150	> 150	60
9T_NVTR	> 200	> 300	60
12T_*	> 300	> 600	60
12T_NVT_R	> 400	> 700	130
18T_LVT (ENC)	> 1420	> 1420	60

Fig. 1.10 Degradation of the speed of a standard cell library inverter in different track width for low-, normal-, and high-Vt implementations. Different widths of standard cell library transistors affect the degradation

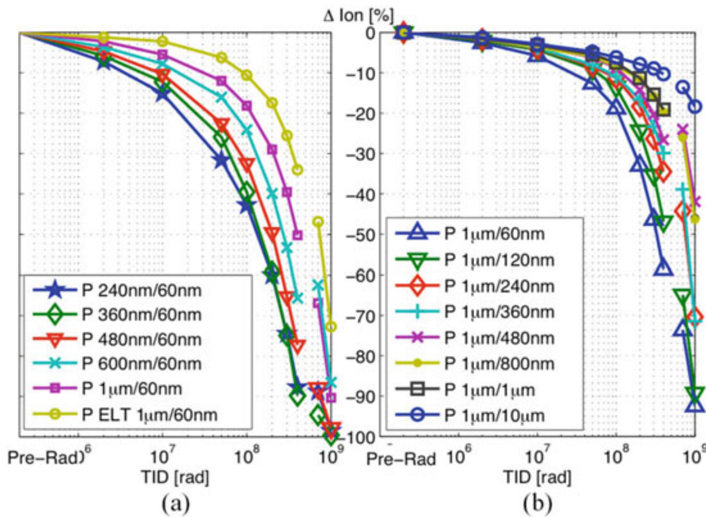


Fig. 1.11 On current of pmos transistors with different geometries: (**a**) Effect of width (**b**) Effect of length

Nmos devices show a significantly better response than pmos devices as can be seen in Fig. 1.12 [24]. For narrow channel effects, one can observe a slight increase in the current at low doses. This originates from the positive trapped charges in the STI as they improve the channel's charge. At higher doses, interface traps become

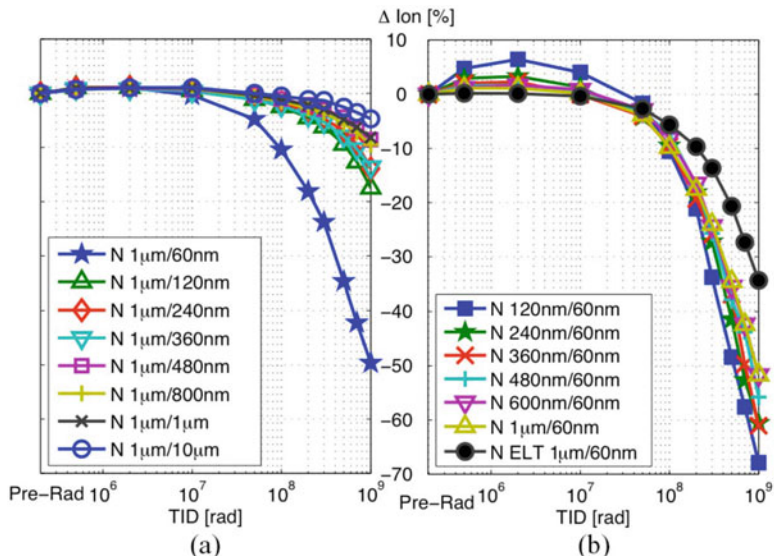


Fig. 1.12 On current of nmos transistors with different geometries: (**a**) Effect of width (**b**) Effect of length

dominant reducing the current in narrow devices. For short devices, the degradation originates from increasing hot carrier damage.

Figure 1.13 [24] shows a comparison between nmos and pmos devices with $L = 120\,\text{nm}$ and $W = 1\,\mu\text{m}$ which is approximately twice the minimum gate length. This demonstrates that nmos transistors are significantly more radiation tolerant than pmos devices in this technology.

1.3 Single-Event Effects

1.3.1 Basic Mechanism

Single-Event Effects (SEEs) are short-term radiation effects in the silicon. Single ionizing particles can ionize the silicon and generate electron-hole pairs as described before. While TID effects originate within the oxides, SEE mechanisms happen in the silicon [25]. The number of collected charges which were generated by the high-energy particle depends on the location of the hit. The highest collection happens when the charges are generated near the junctions of the MOS device. Figure 1.14 shows the process of an SEE hitting the silicon near the drain/source junction of a nmos transistor. After the electron-hole pairs are generated, they are separated by the high electric field in the depletion layer of the junction. When this happens, the separated charges in their turn even extend the electric field beyond the depletion

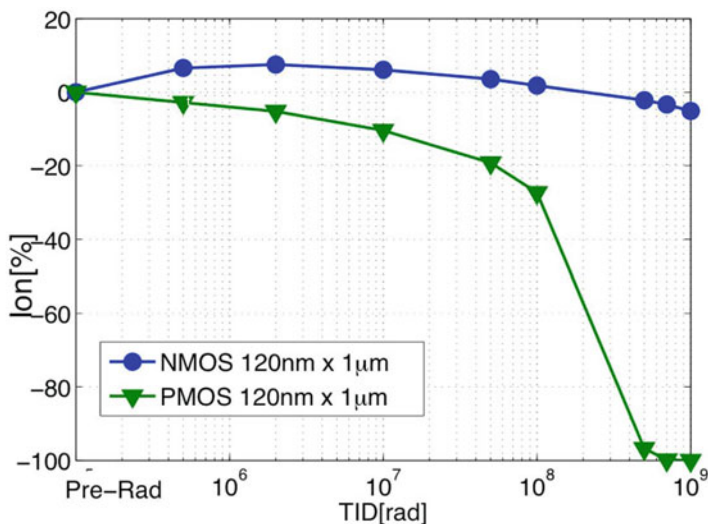


Fig. 1.13 Comparison between the current degradation in nmos and pmos transistors

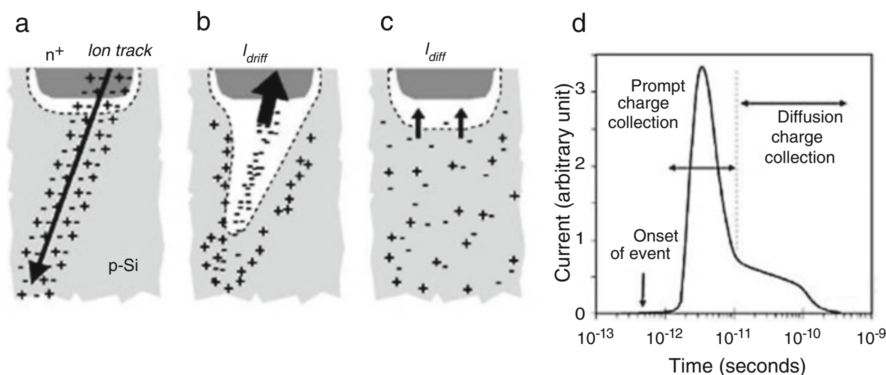


Fig. 1.14 (**a**) Ionizing particle creates electron-hole pairs in the silicon. (**b**) Electrons drift towards the n+ junction creating a funnel. (**c**) The remaining electrons and holes diffuse and recombine

layer resulting in a so-called "funnel" which can be seen as a local depletion layer. The majority of the electrons which do not recombine drift towards the n+ implant which results in a high transient current in the drain or source terminal.

When the electron-hole pairs are being separated, the funnel starts to reduce. The remaining charges which are not transported through drift will be mobilized through diffusion, which is much slower compared to the drift mechanism.

This explains the typical current waveform seen from SEEs as is shown in Fig. 1.14c. The high peak originates from drift while the longer trails originate from diffusion.

These currents are typically modeled with a double exponential Gaussian function [26]:

$$I(t) = Q\frac{e^{t/\tau_1} - e^{t/\tau_2}}{\tau_2 - \tau_1} \quad (1.4)$$

in which Q is the total charge which is collected and τ_1 and τ_2 are the time constants of the rising and falling edges. Typically, τ_1 is 10–50 ps and τ_2 rises beyond 100–200 ps. The total collected charge is difficult to predict since it highly depends on the location of the impact, doping levels, recombination rates, and the potential distribution (electric field) in the device [27].

1.3.2 Effect on nmos and pmos Devices

As discussed, in nmos devices, electrons are captured by the source/drain implants which results in a current from the source/drain junctions into the substrate/bulk contact of the device. The operation is reversed in pmos devices in which holes are captured by the p+ drain/source junctions. This leads to a current from the nwell connection to the drain/source connections as is shown in Fig. 1.15. Typically (especially in digital circuits), nwells are tied to the supply voltage while the substrate is biased at a ground potential. This results in a simplified conclusion that nmos devices drain current to the substrate from a sensitive node while pmos transistors source current to the sensitive node.

A CMOS inverter is shown as an example in Fig. 1.16. The output node is a sensitive node since it is connected to the drains of the nmos and pmos. However, when the output is a logic 0, transient currents from the nmos can never result in a 0 to 1 transition in the logic. This can only originate from a pmos device. The opposite holds true for a 1 to 0 transition.

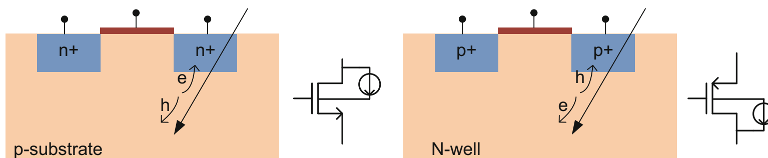


Fig. 1.15 In nmos transistors, electrons drift towards the source/drain junctions leading to a sinked current to the source/drain. In pmos transistors, holes drift towards the source/drain junction leading to a sourced current to the source/drain

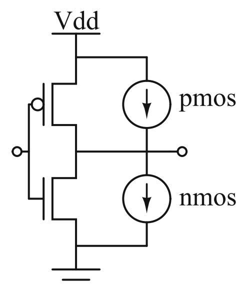


Fig. 1.16 In a digital logic CMOS cell, pmos transistors can only source current to the output node while nmos transistors can only sink current from the output node. Therefore, SEEs on nmos devices can create a 1–0 transition but not a 0–1 transition. The inverse is true for pmos devices

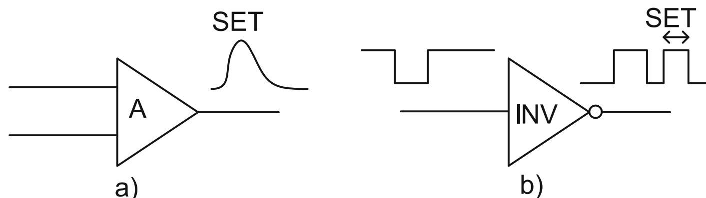


Fig. 1.17 (**a**) SETs on analog devices like amplifiers create temporary signal disturbances which lead to a dramatic reduction in SNR. In most cases, the signals cannot be used anymore. The shape of the SET may also be dependent on the impedance of the node. (**b**) In digital circuits, an SET leads to a temporary inverted bit flip in the logic

1.3.3 SET, SEU, SEL

Single-Event currents can lead to various errors in the circuits. Depending on the type of effect they have, they can be generally divided into 3 major types. Single-Event Transients (SETs), Single-Event Upsets (SEUs), and Single-Event Latchup (SEL).

SETs are transient voltages and currents which originate from the currents generated by the charged particle. In analog circuits, this leads to current and voltage transients in the circuits which may temporarily disturb the operation of the signal. Figure 1.17a shows an example of an SET occurring in an analog circuit. The SET can be seen as an excess noise source with extremely high amplitude. It may not only be significantly larger than the signal but it may also disturb the biasing point of the circuit which needs some time to recover. In digital circuits, as is shown in Fig. 1.17b, an SET generates a temporarily wrong digital value [28]. When an SET occurs in a sequential digital logic within the setup and hold times of the registers, the SET may be captured which leads to an incorrect logical state.

The sensitivity of a digital sequential block to SETs is typically dependent on three parameters. Firstly, the cross section of the logic cells which describes how much area is sensitive to the radiation. Secondly, when the clock frequency increases, the probability of capturing an SET is also increases. And thirdly, due to bit masking, not all SETs propagate to the input of a register [29]. Typically, the bit masking in digital designs approximates 40 %. The overall cross section of the

design that is sensitive to SETs can be calculated as

$$\sum X_{cell} A_{mask} \frac{T_{setup+hold}}{T_{clock}} \tag{1.5}$$

in which X_{cell} is the cross section of a logic cell, A_{mask} is the digital bit masking, $T_{setup+hold}$ is the setup and hold time of the end point, and T_{clock} is the clock period.

SEUs are errors in digital circuits which have a memory-like register behavior like latches and flip-flops. When the register involves a bit-flip, this erroneous number may remain in the digital block and may even propagate to other digital modules [30]. For example, an SEU may change the state of an FSM temporarily. SEUs can originate from direct upsets in the registers but may also be a result from SETs in the combinational logic. In large on-chip SRAM memories, SEUs can severely corrupt the data in the memory. Therefore, typically scrubbing and error correction is done to refresh the memories.

CMOS technologies on silicon substrates are known to be prone to latch-up. This effect occurs due to parasitic combined bipolar transistors which originate between nmos and pmos transistors. The combined bipolar structure can be in a positive feedback state once triggered such that a DC current flows from the supply to the ground terminal. Once triggered, the only way to stop the latch-up is to cut the power supply. Generally, latch-up can be triggered through transient currents, in the PNPN structure. This is exactly what occurs when an ionizing particle passes through the chip [31]. This effect is known as Single-Event Latch-up. Latch-up can be avoided by design by ensuring small substrate resistances and wide spacing between pmos and nmos devices. However, in the technologies used in this work, SEL has not been observed for a minimum sized spacing between nmos and pmos devices in digital standard cell libraries.

These effects are all non-destructive (however, SEL can be destructive if the current density becomes too high). Single-events can also be destructive like Single-Event Burnout (SEB) and Single-Event Gate Damage (SEGD) [32] but these are not further discussed here.

Note that also non-nuclear applications cope with single-event soft errors with shrinking technology nodes [33].

1.3.4 SEU Mitigation Techniques in Digital Blocks

Digital circuits are the most easy to harden against SEEs [6]. A common and highly efficient way of ensuring correct behavior is the implementation of Triple Modular Redundancy (TMR). In a TMR circuit, all logic is implemented three times and voters are employed to correct single errors in the logic. Multiple implementations of TMR are possible depending on the available recourses [34]. The most complete form, and also the most robust is shown in Fig. 1.18. This is a general form of digital sequential logic. Both the logic and the registers are triplicated and cross-checked

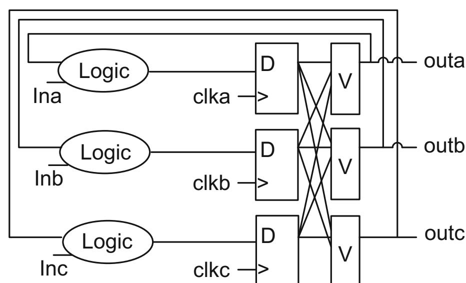


Fig. 1.18 Fully TMR structure with triplicated registers, logic, voters, and clock tree

by three voters. In case of any single error in the logic or the registers, all registers will be corrected in the next clock cycle. This technique works if there is only one error in the logic feedback path within a clock cycle. However, the probability of two upsets at the same location by different particles is extremely small. With shrinking technology nodes, the effects of multi-bit upsets become more important and may need to be addressed separately in the future. It may require different placement strategies that take into account multi-bit upsets in the logic. Note that also the clock trees for the registers are triplicated since SETs can also occur in the clock tree.

While this technique is extremely robust against SEEs, its main drawback is the power consumption and area consumption which is more than three times larger. Also, the digital timing is degraded due to the additional voters and larger routing overhead within the circuit.

Various simplified topologies, originating from this structure can be implemented which improve the area efficiency, power consumption, or speed at the cost of higher SEU cross section. For example, the triplicated clock trees can be combined in one clock tree which saves power since a lot of power is typically consumed in the clock tree. Furthermore, the combinational logic can be simplified to only one instance. As explained before, SETs in the logic depend on the propagation probability and are only captured when they happen within the setup and hold times of the flip-flop. A simplified TMR implementation may save power and area at the cost of single-event sensitivity. In this case, the design should tolerate errors at a system level since it is not fully protected.

Finally, a regular logic implementation can be used with radiation hardened flip-flops which are designed to be tolerant SEEs. For example, DICE latch based flip-flops as shown in Fig. 1.19 use interlocked nodes to correct SEUs in the latch [35]. In this circuit, nodes X1 and X3 are the inverse of nodes X2 and X4. Any upset in X1-4 will be compensated by the other nodes. Another technique which is widely used in industry is time-protected flip-flops [36]. Also, triplicated self-correcting latches are used which immediately correct themselves after an error is detected without the need to wait for a new clock cycle as is the case in regular TMR. The main disadvantage of these techniques is the need to design a custom standard cell

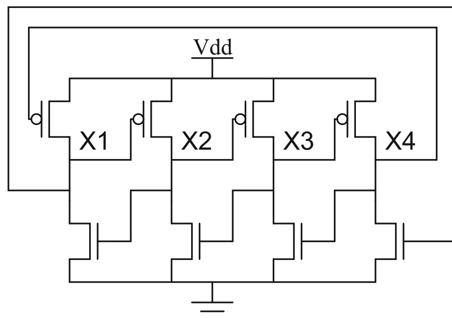


Fig. 1.19 DICE latch with four interlocked nodes

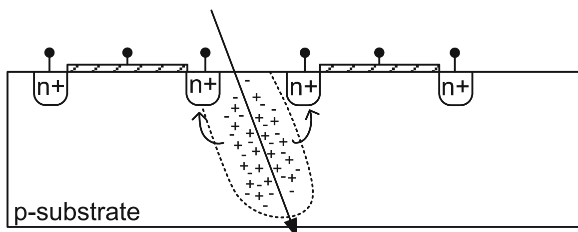


Fig. 1.20 Charge generated from a single particle can extend up to 10 µm such that it can be collected by multiple junctions. The amount of charge sharing depends on the position and reverse junction voltage of both junctions

library and extract the correct timing for digital place & route tools which may be time-consuming and expensive.

Note that TMR can be automatically generated from a HDL digital design [37].

1.3.5 Charge Sharing

The charges generated in the chip are typically generated in a diameter of 1 µm up to 10 µm perpendicular to the particles' trajectories [38]. In deep submicron technologies, this charge distribution may influence different junctions or even different transistors as is seen in Fig. 1.20 [39]. In digital circuits, multiple cells or registers may be upset simultaneously leading to Multiple-Bit Upsets (MBUs). Generally, MBUs are not disastrous when triplication techniques are used. However, TMR relies on the fact that only one bit is upset from a common register. To ensure a correct TMR operation, the three common registers (representing 1 logical bit) should be spaced enough to reduce the chances of MBUs. This can be automatically ensured in place & route tools.

In analog circuits, this effect can even be exploited to improve the radiation hardness of a circuit. For example, if the drains of a differential amplifier's input pair are closely spaced to each other, the collected charge will be shared between the nodes leading to a common mode component of the SET which will have less influence on the signal. In general, if an optimized common centroid layout is used in differential analog circuits, this effect can be exploited which is discussed in detail in [38].

1.4 Simulation Methods to Simulate Radiation Effects

Simulating radiation effects can be a challenge in complex systems. Depending on the hierarchy, system level failures can be simulated such as fault tolerance and fault propagation. At low level devices, where this work is focusing on, the goal is to find sensitive blocks in the design and the circuits. To investigate the influence of radiation on the circuit performance, simulation methods can be divided into TID effects and SEU effects.

1.4.1 Simulation of TID Effects on Circuits

TID effects are cumulative effects on the devices and degrade the devices in the circuit. As discussed before, it has become difficult to model the TID radiation effects on the nanoscale devices. A general way to model radiation effects during simulation is to extend the corners of the process in an extra dose dimension. For a given technology, the devices are characterized at different doses for different device sizes that may be available since the geometry of the devices has significant influence on the radiation sensitivity. Thus, the transistor parameters in the models are adjusted for different doses which is done experimentally. An extrapolation can be performed for different process corners in the technology.

The major challenge in this method is to correctly extract the model parameters of the devices which were measured in the experiment. Typically only device currents are measured experimentally from which other model parameters (such as channel mobility and threshold voltage) should be extracted. Figure 1.21 shows a schematic representation of the parameter extraction from a TID experiment. Before radiation, the parameters (like Vt) are known and spread over different process variations. A batch of samples, usually in a typical corner, is irradiated and measured at discrete doses. The variation can then be interpolated for different doses and extrapolated to different corners if time and budget does not allow irradiation campaigns on various process corners. Note that the dose itself does not only determine the

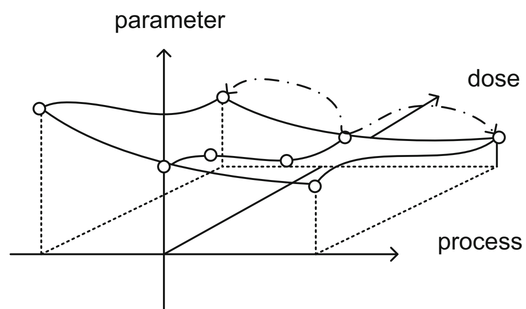


Fig. 1.21 Parameter model as function of process variations and dose

damaging effects but also the dose-rate, temperature, and node voltages have an effect on the radiation damage. These parameters will be additional dimensions in this model.

1.4.2 Simulation of Single-Event Effects on Circuits

SEU effects are intrinsically different from TID effects since the timescale is different and the effect is not accumulating. Once the correct parameters are extracted from TID experiments, the simulation method is straightforward as an extra corner dimension. TID effects can be assumed to be uniform for the different devices on the same chip which is not the case for single-event effects as they happen for only some fraction of time locally.

In digital circuits, SEU effects can be estimated by fault injection methods. In digital simulators, random bit-flips and transients can be inserted to investigate if the system is sensitive to the upsets.

In analog blocks, the amount of charge captured by the devices can be important since it disturbs analog valued signals, also the shape of the SEE current should not be neglected. These shapes can be estimated from TCAD simulations which can calculate charge mobility in the devices after a particle has hit the chip [40]. The amount of charges and the interaction of the particle with the silicon can be estimated from Monte-Carlo nuclear simulators like GEANT4 [41] and FLUKA. These are tools which are developed at CERN to simulate the interaction between different radiation sources and material geometries. The output of these tools are 3D (or 2.5D) energy depositions of the particle in the silicon from which the amount of electron-hole pairs being generated can be calculated. This data can be used in TCAD to simulate voltages and currents in basic circuits with few transistors. To simulate the analog blocks in a larger system, the transients should be modeled to behavioral models of the components. Figure 1.22 shows a schematic on the

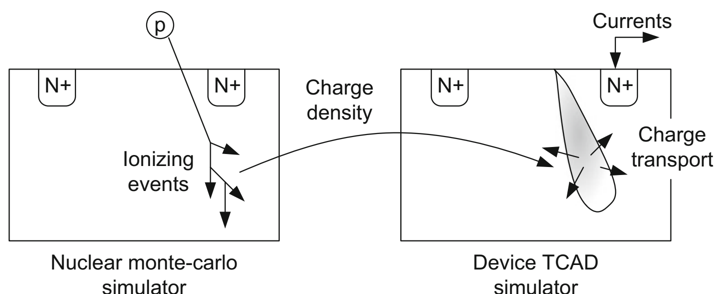


Fig. 1.22 Monte-Carlo particle interactions estimate energy deposition in ionization events in the silicon substrate from which charge generation can be estimated. The charge density distribution is the initial state of carrier generation for the TCAD model

SEU simulation for spice input. In the first step, MC nuclear simulator estimates the spatial energy deposition and charge densities which are initial states for the TCAD simulator. The output of this flow are currents at the device nodes which can be used in spice simulations [42]. Note that this simulation way is very time-consuming and is an estimation for the reaction of the circuit to the charges since correct TCAD models cannot be constructed since the foundry information is not made available. Therefore, this flow is used to understand the mechanisms how the circuits react to the charges and not as a formal verification of the device performance. Radiation assessment is still required for the devices before they can be qualified for applications in radiation environments.

These methods can be time-consuming and impractical in many designs. As discussed before, the current pulses can also be modeled as a double exponential function [26].

1.5 Conclusion

Long term, accumulating radiation effects are observed, even in advanced CMOS technology nodes. While they were originally observed in the gate-oxide, TID effects today are seen in secondary oxides such as STI and LDD spacer oxides. In 65 nm CMOS technology nodes, it has been seen that pmos transistors degrade significantly more than nmos devices. Also, TID effects were observed to be significantly geometry dependent such that short and narrow transistors degrade more than long and wide transistors.

Single-Event Effects become even more important in shrinking technologies as the node capacitances are decreasing. Ionizing particles generate temporary disturbing charges and currents in the circuits which may lead to transient voltages and incorrect digital values. The charges are collected at the device junctions. While charge sharing can occur between different nodes, triplicated structures are a common approach to mitigate SEEs in digital modules at the cost of power and area.

While radiation cannot be directly included in SPICE simulations, an approximation through Monte-Carlo simulations and TCAD models can be made to estimate the currents generated in the devices to simulate the effect on the circuits. TID effects were known to be successfully included as additional dimension in the corners of the technology.