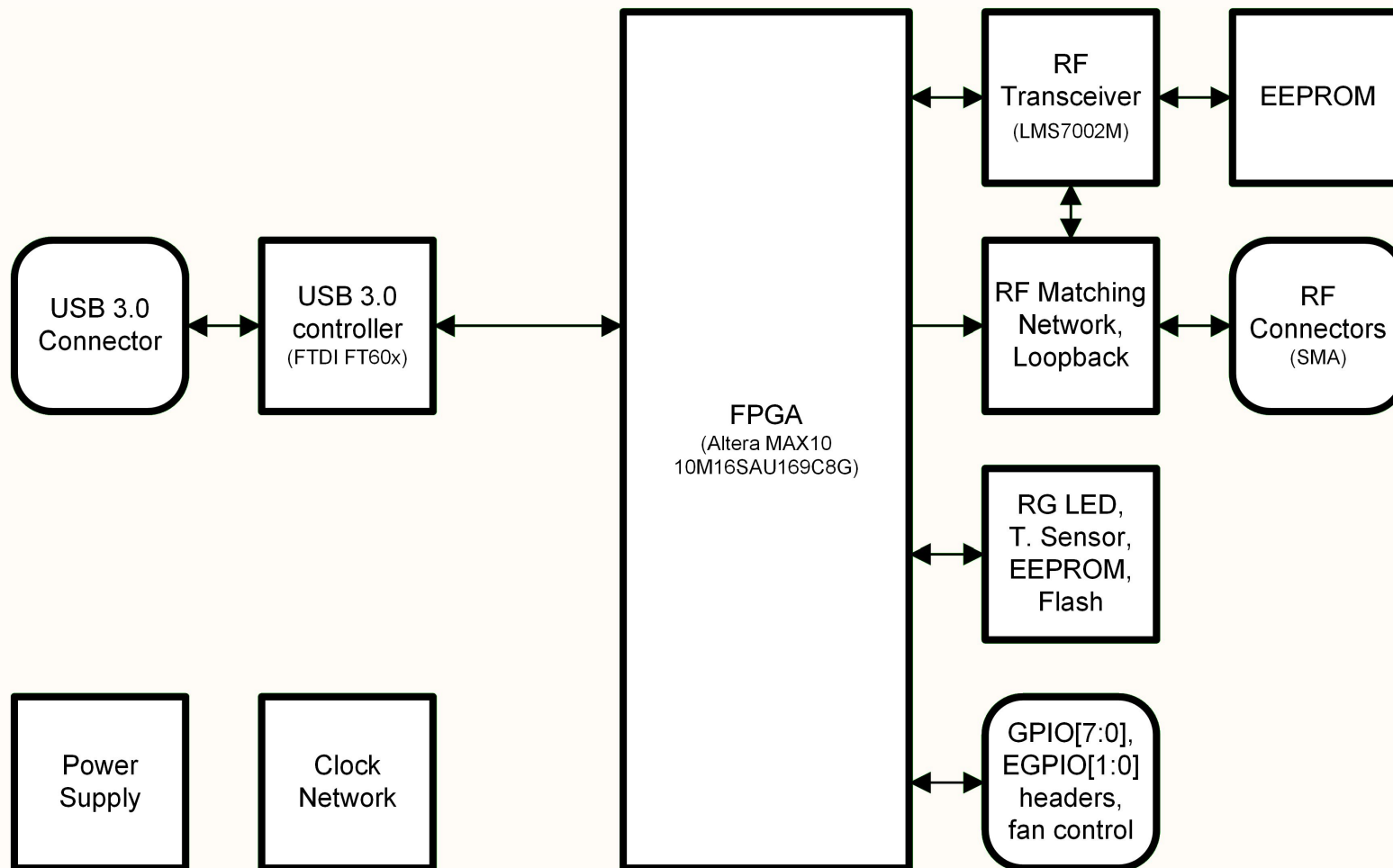


Block diagram



Project name: **LimeSDR_Mini_v1.PrjPcb**

Title: **Block diagram**

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom

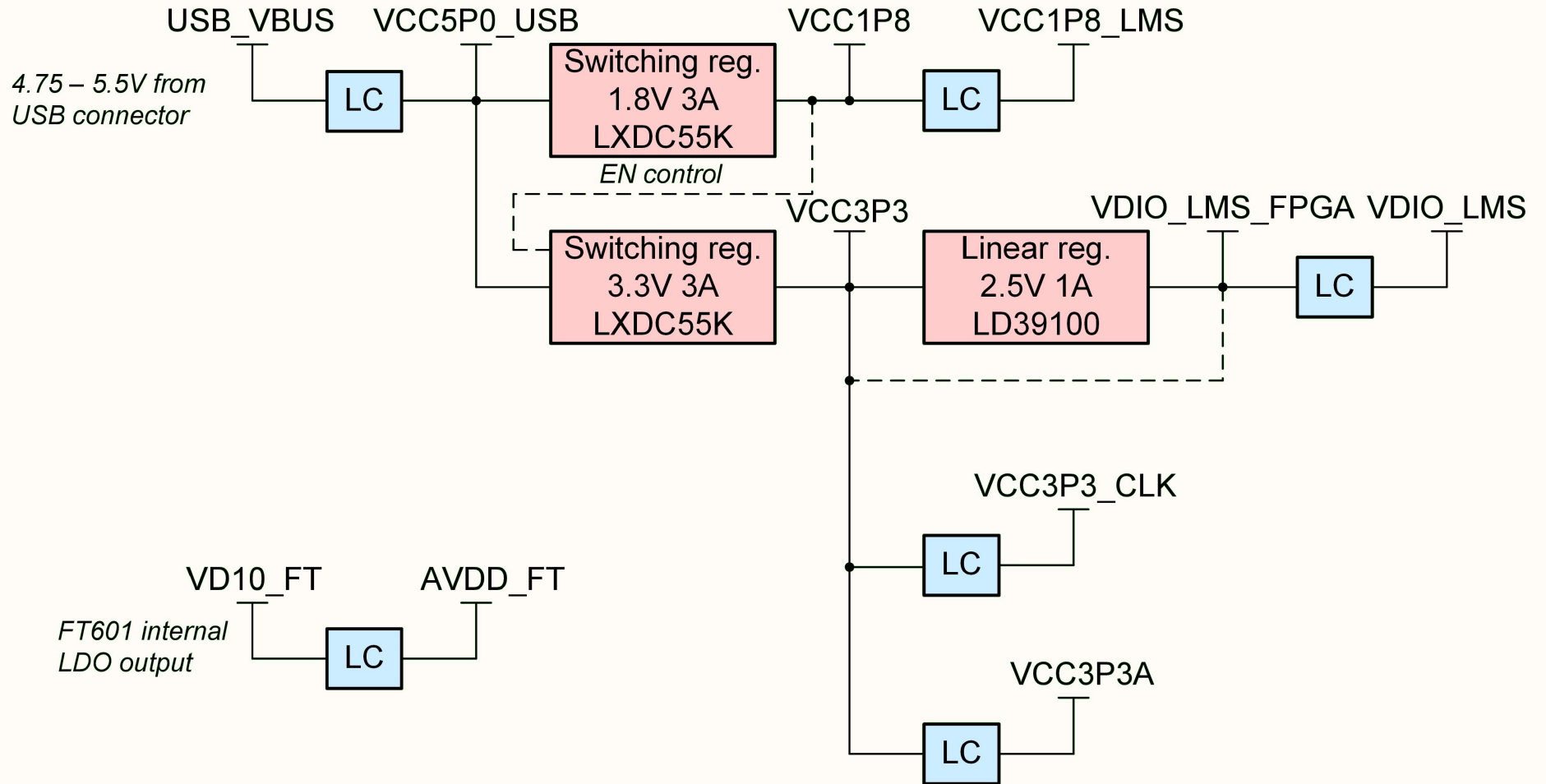



Size: **A4** Revision: **v1.1**

Date: 2017-12-11 Time: 17:51:03 Sheet 1 of 9

File: 01_BlockDiagram.SchDoc

Power diagram

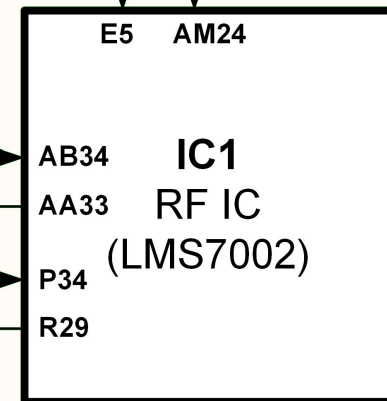
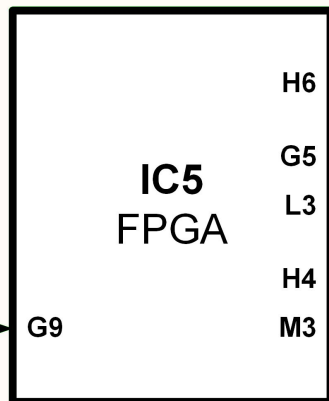
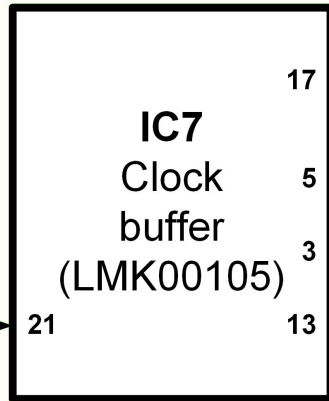
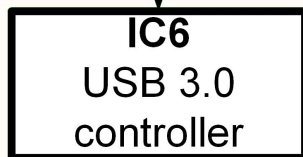
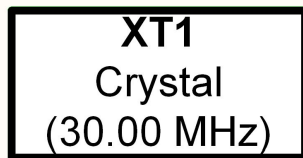
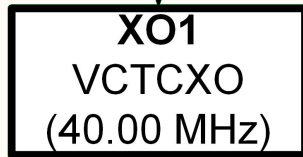


Project name: LimeSDR_Mini_v1.PrjPcb		
Title: Power diagram		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: A4	Revision: v1.1	
Date: 2017-12-11	Time: 17:51:06	
File: 02_PowerDiagram.SchDoc		

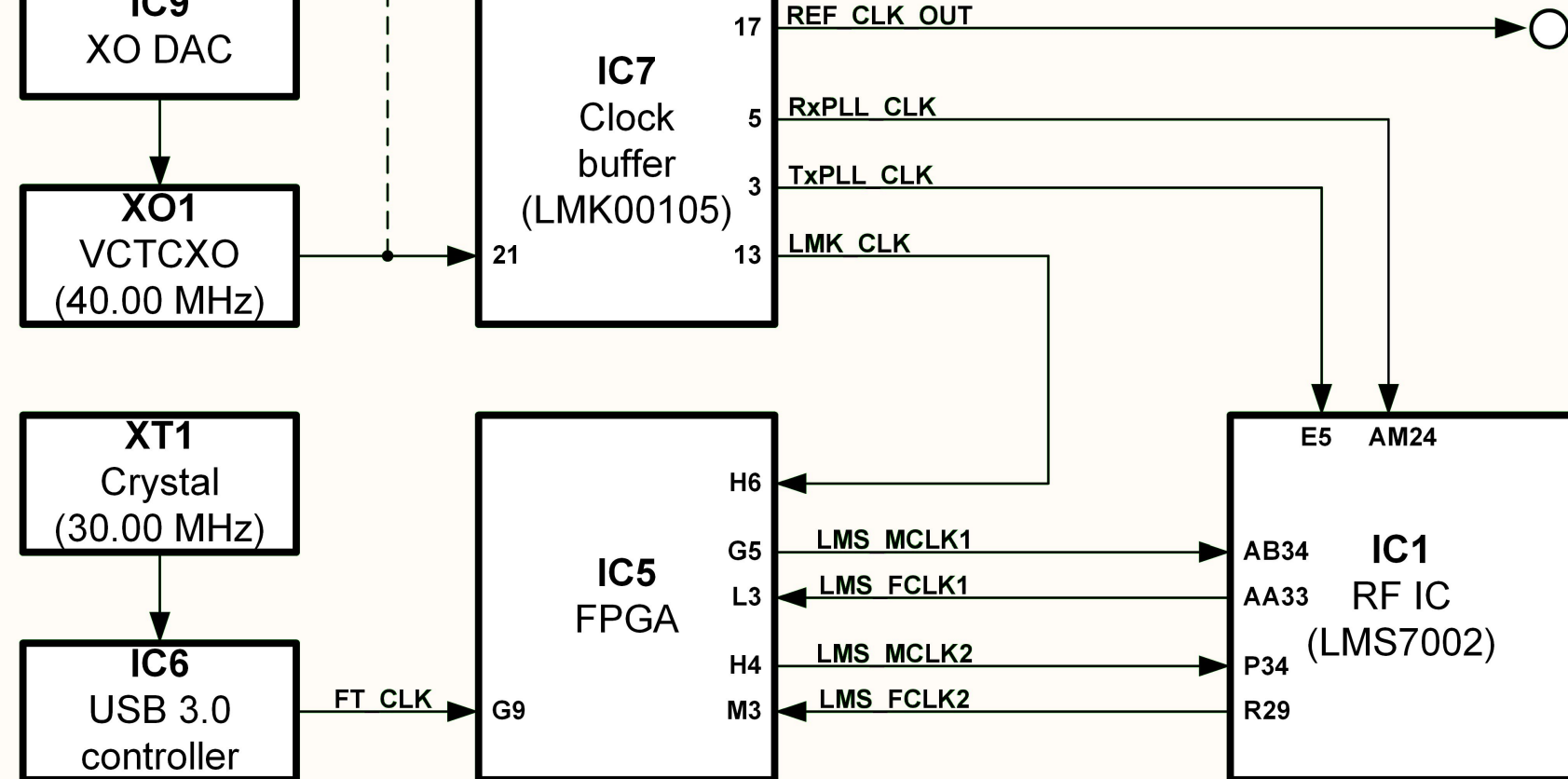
Clock diagram


J8 U.FL connector

REF CLK IN



J9 U.FL connector

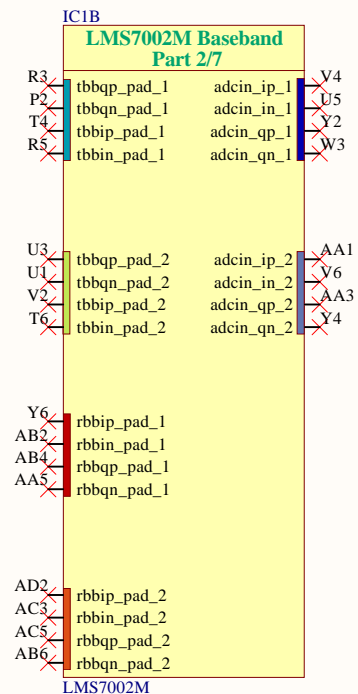
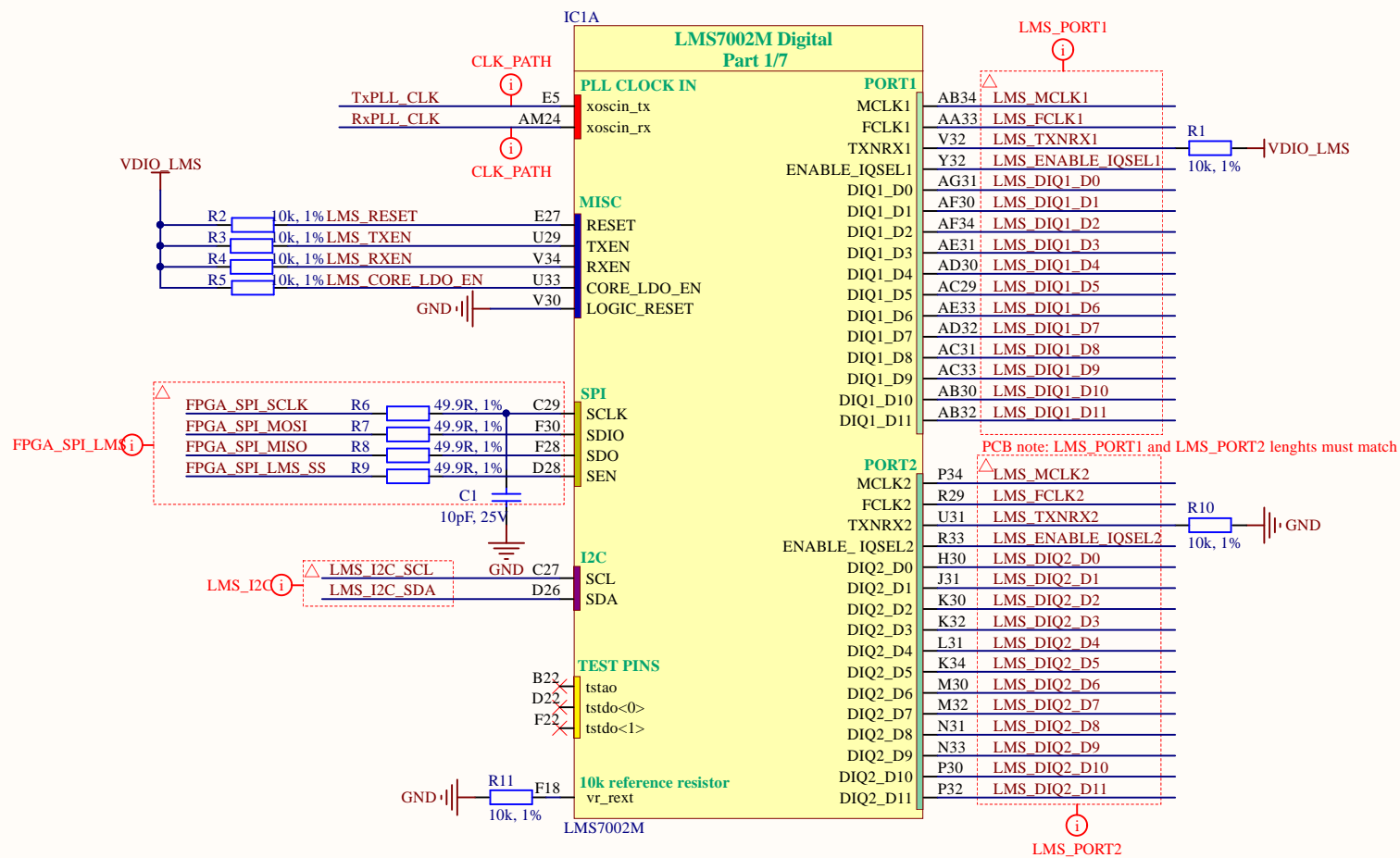


Project name: <i>LimeSDR_Mini_Iv1.PrjPcb</i>		
Title: <i>Clock diagram</i>		Lime Microsystems Surrey Tech Centre Guildford GU2 7YG Surrey United Kingdom
Size: <i>A4</i>	Revision: <i>v1.1</i>	
Date: <i>2017-12-11</i>	Time: <i>17:51:09</i>	
File: <i>03_ClockDiagram.SchDoc</i>		

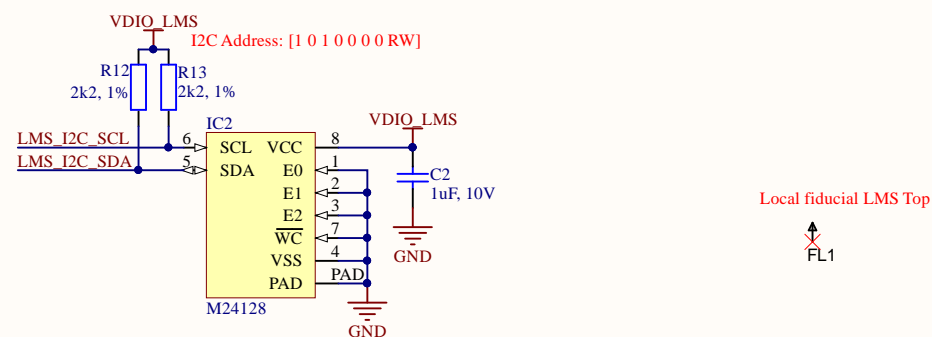
LMS7002M misc

LMS7002M digital circuit

Baseband external IO



LMS EEPROM

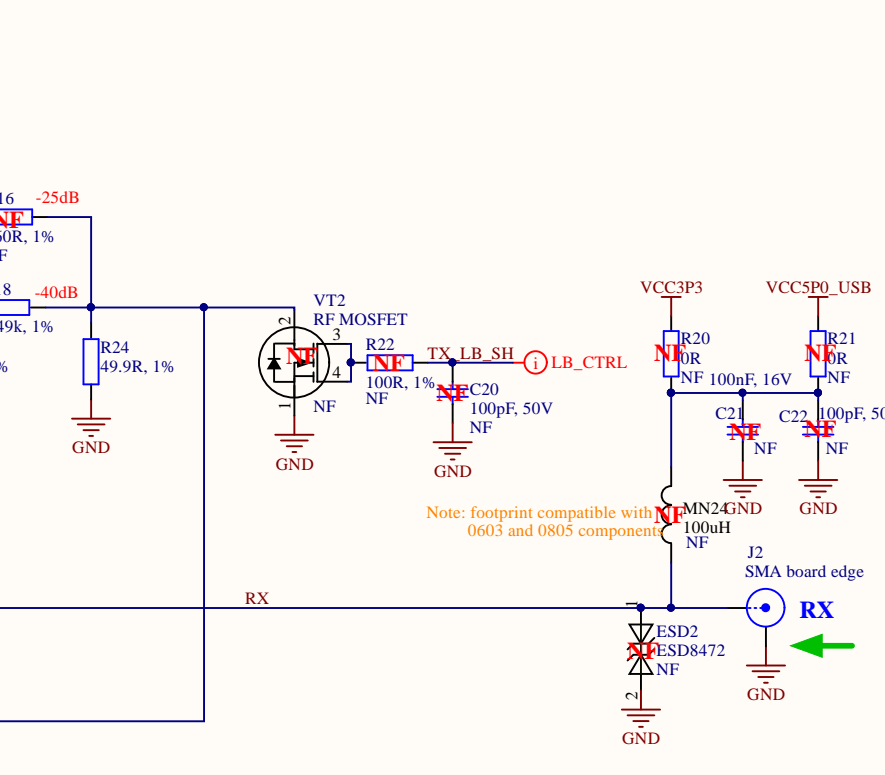
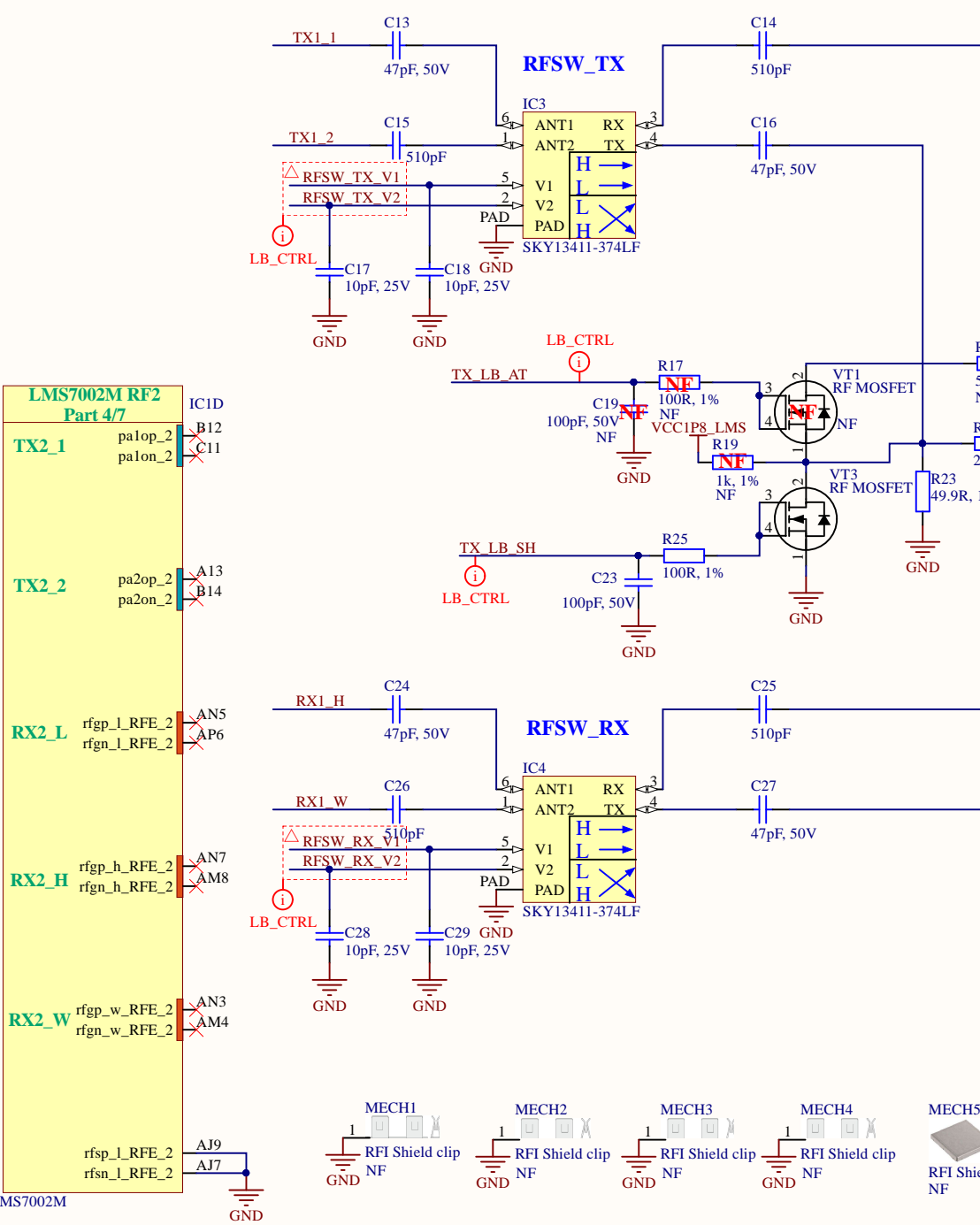
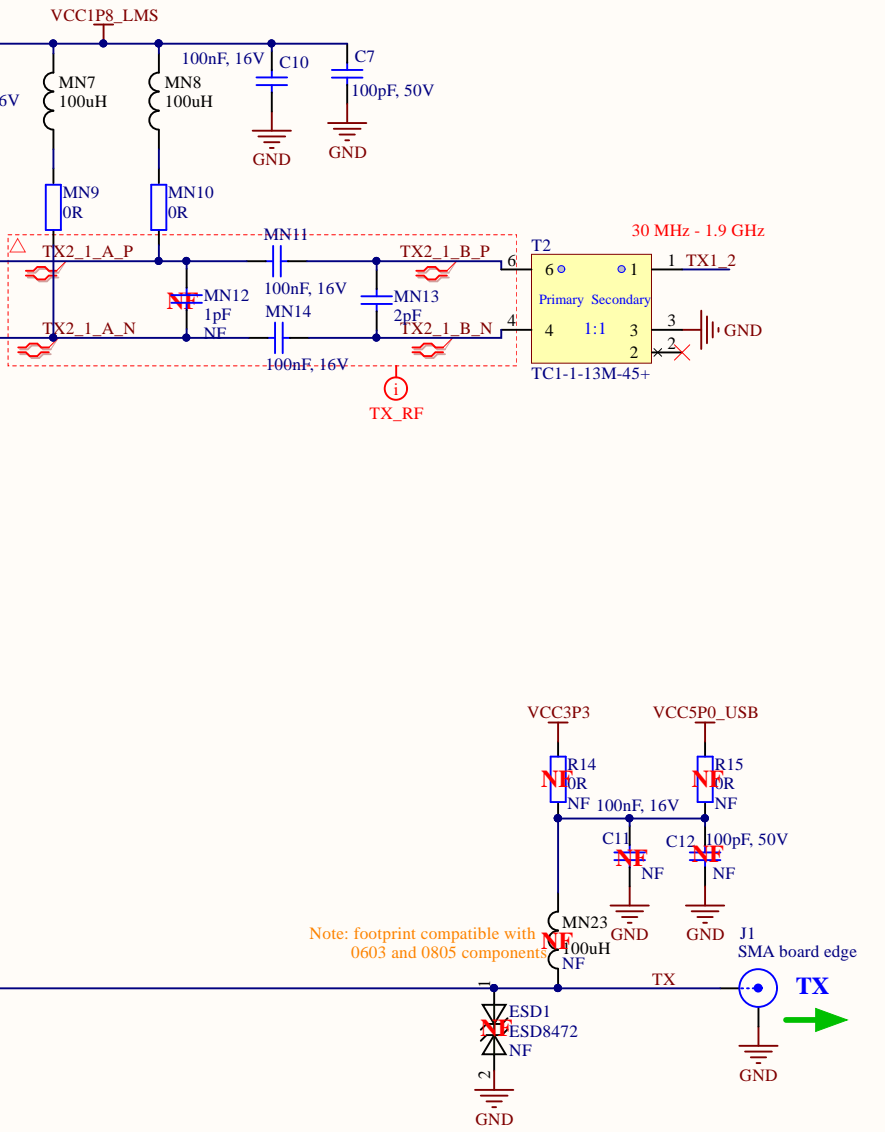
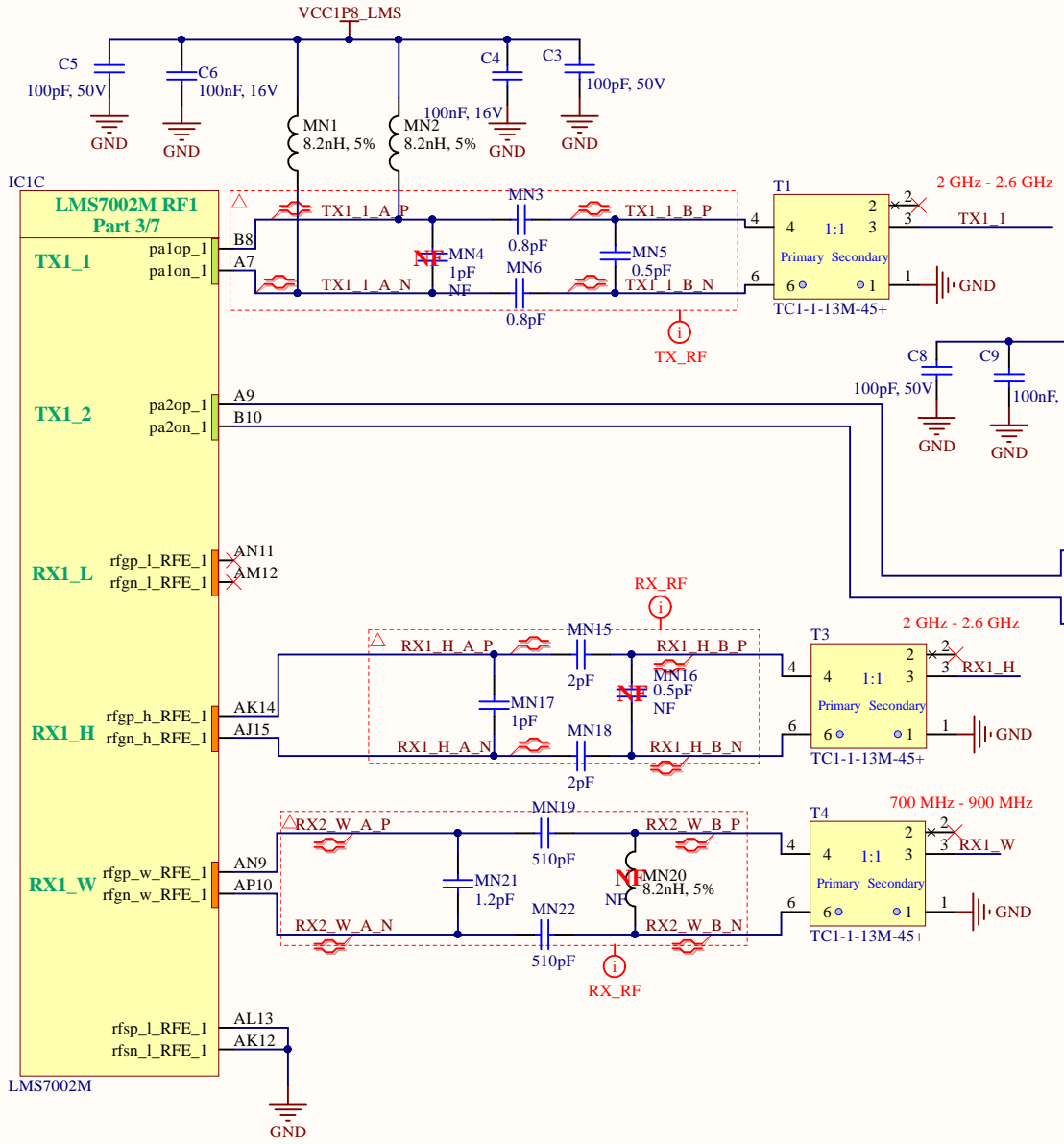


LMS7002M RF circuits

LMS RF Channel 1

RF truth table

RFSW_TX		RFSW_RX		J1	J2	Loopback
V1	V2	V1	V2	(TX)	(RX)	
H	L	H	L	TX1_1	RX1_H	TX1_2 → RX1_W
L	H	H	L	TX1_2	RX1_H	TX1_1 → RX1_W
H	L	L	H	TX1_1	RX1_W	TX1_2 → RX1_H
L	H	L	H	TX1_2	RX1_W	TX1_1 → RX1_H



RFSW (SKY13411) truth table

V1	V2	ANT1 → TX (pin 6) → (pin 4)	ANT1 → RX (pin 6) → (pin 3)	ANT2 → TX (pin 1) → (pin 4)	ANT2 → RX (pin 1) → (pin 3)
H	L	ISOLATION	ON	ON	ISOLATION
L	H	ON	ISOLATION	ISOLATION	ON

LMS7002M power supply circuit

IC1E

LMS7002M Power Part 5/7

1.8V Digital
VDD18_DIG

1.8V-3.3V Digital
DIGPRVDD2
DIGPRVDD2
DIGPRVDD2
DIGPRVDD2
DIGPRPOC

1.8V Analog
VDD18_VCO_SXT
VDD18_LDO_TX
VDD18_TIA_RFE
VDD18_LDO_RX
VDD18_SXR
VDD18_VCO_SXR
VDD18_BIAS
VDD18_TRF
VDD18_VCO_CGEN

1.8V-3.3V Analog
VDD18_TXBUF
VDD18_RXBUF

LMS7002M

IC1F

LMS7002M Power Part 6/7

1.25V Digital
DIGPRVDD1
DIGPRVDD1
DIGPRVDD1
DIGPRVDD1

DVDD_SXR
DVDD_SXT
VDD12_DIG
VDD_SPI_BUF
DVDD_CGEN

1.25V Analog
VDD12_TXBUF
VDD120_VCO_SXT
VDD12_VCO_SXT
VDD_CP_SXT
VDD_TBB
VDD12_TIA_RFE
VDD12_LNA_RFE
VDD_CP_SXR
VDD_DIV_SXR
VDD12_VCO_SXR
VDD12_RXBUF
VDD_AFE
VDD_CP_CGEN
VDD_DIV_CGEN
VDD_TPAD_TRF
VDD_TLOBUF_TRF
VDDO_TLOBUF_TRF

1.25V-1.4V Analog
VDD_DIV_SXT
VDDO_DIV_SXT
VDD_MXLOBUF_RFE

1.4V Analog
VDD14_RBB
VDD14_TIA_RFE
VDD14_LNA_RFE
VDD14_VCO_CGEN

LMS7002M

IC1G

LMS7002M GND Part 7/7

<table border="0" style="width: 100%;"> <tr><td>N3</td><td>Digital gnd</td><td>Analog gnd</td><td>L3</td></tr> <tr><td>AM22</td><td>DGND_SXT</td><td>GND_DIV_SXT</td><td>K4</td></tr> <tr><td>E25</td><td>DGND_SXR</td><td>GND_CP_SXT</td><td>AN25</td></tr> <tr><td>C23</td><td>GND_SPI_BUF</td><td>GND_RXBUF</td><td>AK20</td></tr> <tr><td>B18</td><td>GND_DIG</td><td>GND_DIV_SXR</td><td>AJ19</td></tr> <tr><td>J33</td><td>DGND_CGEN</td><td>GND_CP_SXR</td><td>B20</td></tr> <tr><td>AA31</td><td>DIGPRGND1</td><td>GND_CP_CGEN</td><td>F6</td></tr> <tr><td>AG29</td><td>DIGPRGND1</td><td>GND_TXBUF</td><td>D20</td></tr> <tr><td>T30</td><td>DIGPRGND1</td><td>GND_DIV_CGEN</td><td>AL23</td></tr> <tr><td>W29</td><td>DIGPRGND1.2</td><td>GND_VCO_SXR</td><td>H2</td></tr> <tr><td>G31</td><td>DIGPRGND1</td><td>GND_VCO_SXT</td><td>C7</td></tr> <tr><td>AF32</td><td>DIGPRGND2</td><td>GND_TLOBUF_TRF</td><td></td></tr> <tr><td>Y30</td><td>DIGPRGND2</td><td></td><td></td></tr> </table>	N3	Digital gnd	Analog gnd	L3	AM22	DGND_SXT	GND_DIV_SXT	K4	E25	DGND_SXR	GND_CP_SXT	AN25	C23	GND_SPI_BUF	GND_RXBUF	AK20	B18	GND_DIG	GND_DIV_SXR	AJ19	J33	DGND_CGEN	GND_CP_SXR	B20	AA31	DIGPRGND1	GND_CP_CGEN	F6	AG29	DIGPRGND1	GND_TXBUF	D20	T30	DIGPRGND1	GND_DIV_CGEN	AL23	W29	DIGPRGND1.2	GND_VCO_SXR	H2	G31	DIGPRGND1	GND_VCO_SXT	C7	AF32	DIGPRGND2	GND_TLOBUF_TRF		Y30	DIGPRGND2			<table border="0" style="width: 100%;"> <tr><td></td><td>Thermal pad</td><td></td><td></td></tr> <tr><td></td><td>EP</td><td></td><td></td></tr> </table>		Thermal pad				EP		
N3	Digital gnd	Analog gnd	L3																																																										
AM22	DGND_SXT	GND_DIV_SXT	K4																																																										
E25	DGND_SXR	GND_CP_SXT	AN25																																																										
C23	GND_SPI_BUF	GND_RXBUF	AK20																																																										
B18	GND_DIG	GND_DIV_SXR	AJ19																																																										
J33	DGND_CGEN	GND_CP_SXR	B20																																																										
AA31	DIGPRGND1	GND_CP_CGEN	F6																																																										
AG29	DIGPRGND1	GND_TXBUF	D20																																																										
T30	DIGPRGND1	GND_DIV_CGEN	AL23																																																										
W29	DIGPRGND1.2	GND_VCO_SXR	H2																																																										
G31	DIGPRGND1	GND_VCO_SXT	C7																																																										
AF32	DIGPRGND2	GND_TLOBUF_TRF																																																											
Y30	DIGPRGND2																																																												
	Thermal pad																																																												
	EP																																																												

GND

LMS7002M

GND

Internal LDOs are used

Project name: **LimeSDR_Mini_1v1.PrfPcb**

Title: **LMS7002M power supply**

Lime Microsystems
Surrey Tech Centre
Guildford GU2 7YG
Surrey
United Kingdom



Size: A3

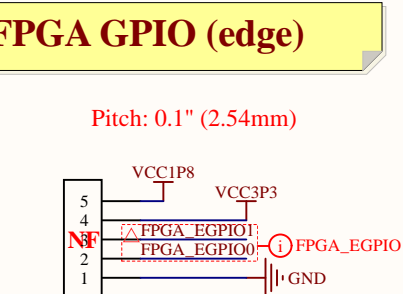
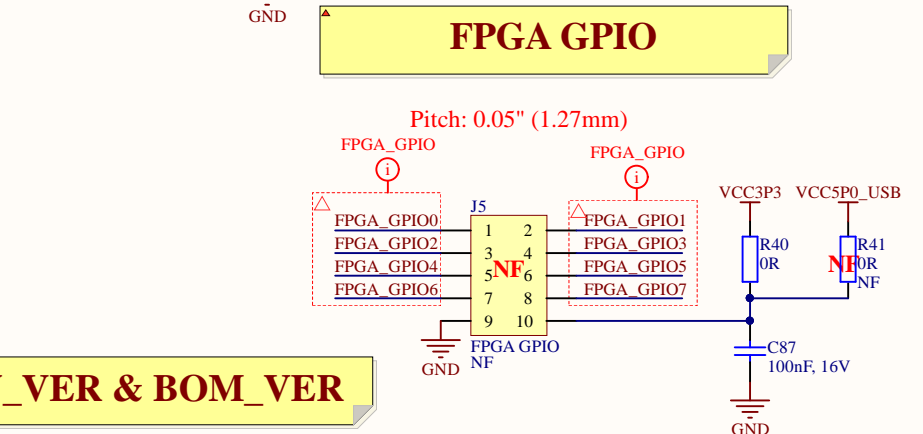
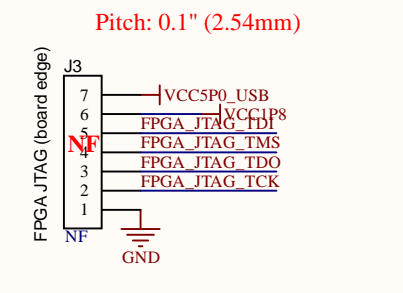
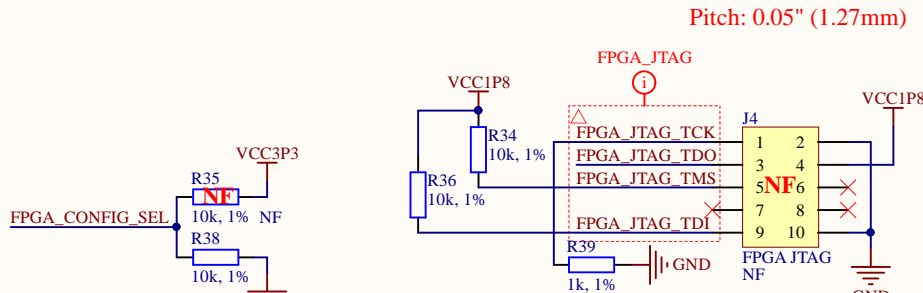
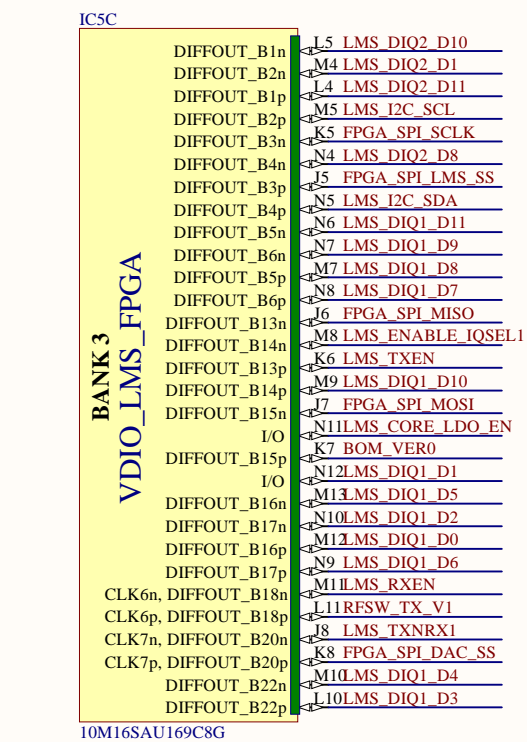
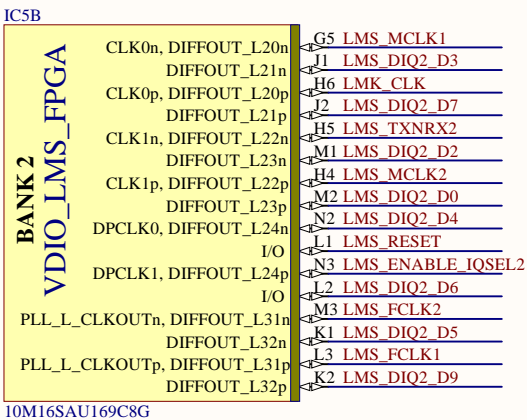
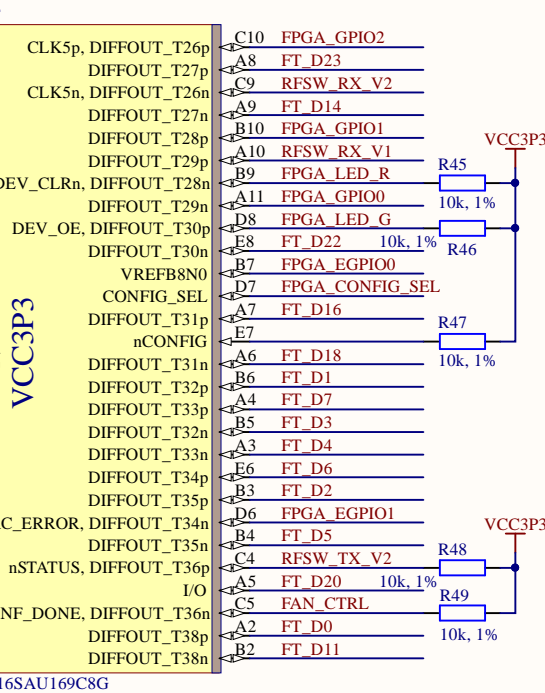
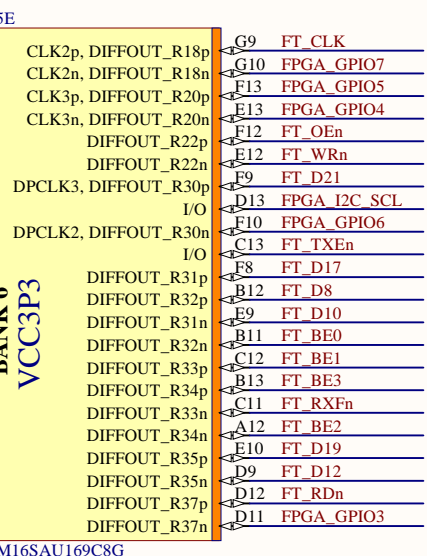
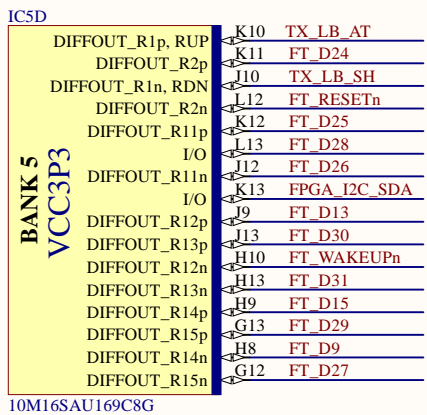
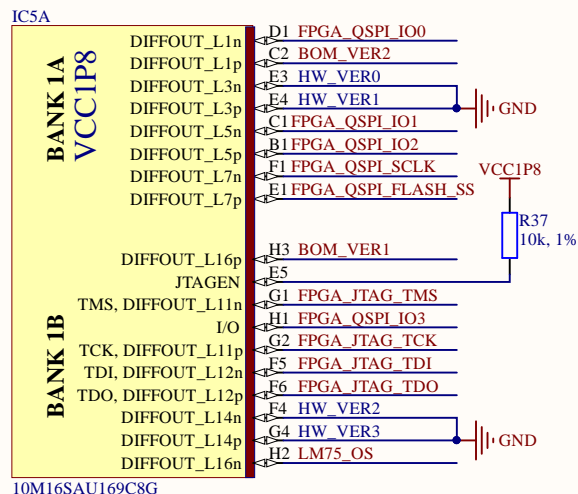
Revision: v1.1

Date: 2017-12-11 Time: 17:51:16 Sheet 6 of 9

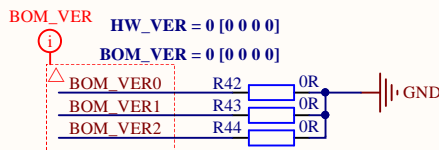
File: 06_LMS7002M_Power.SchDoc

FPGA

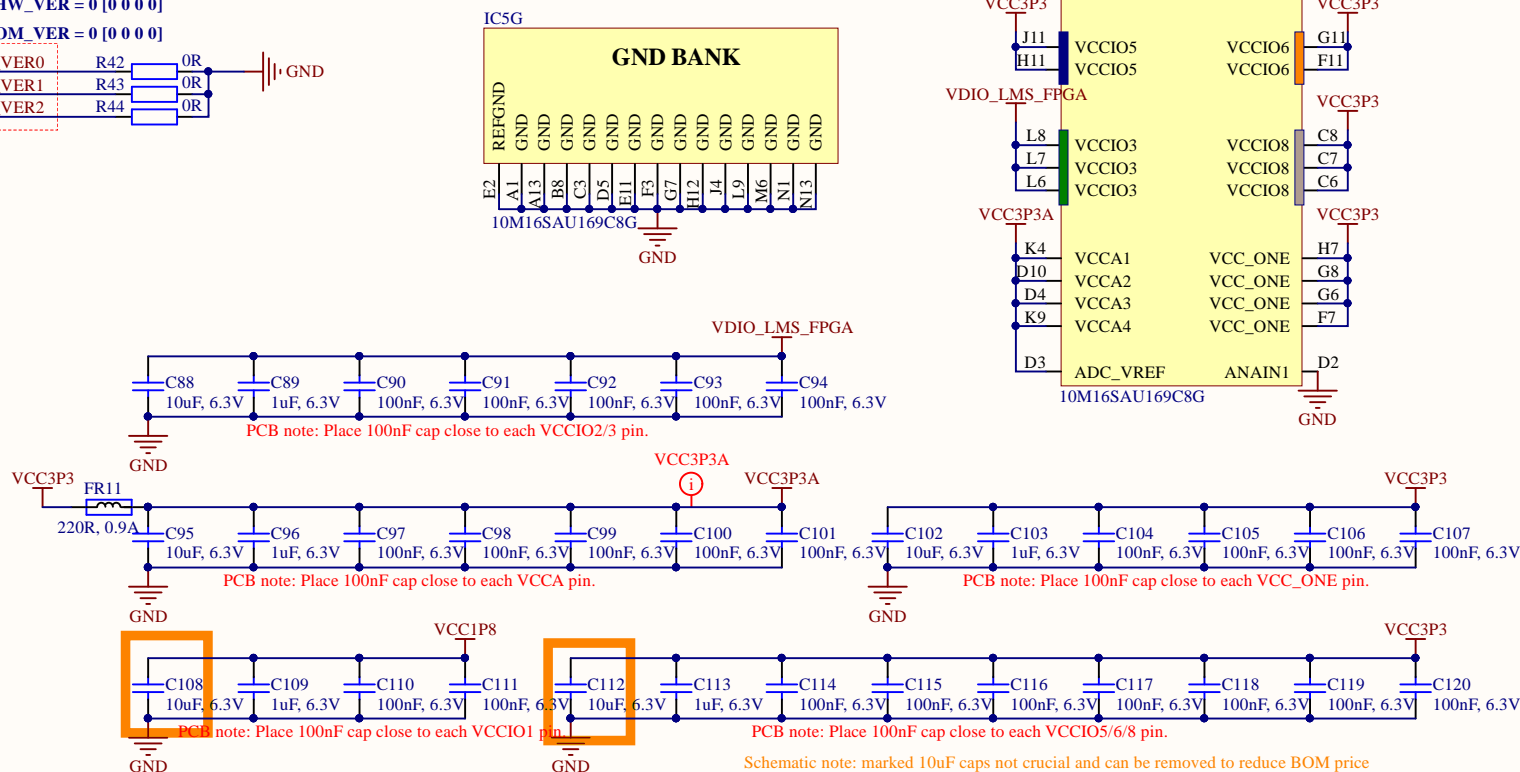
FPGA Banks



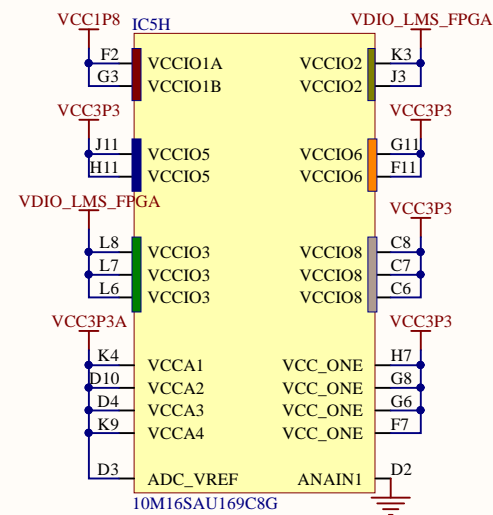
HW_VER & BOM_VER



GND BANK



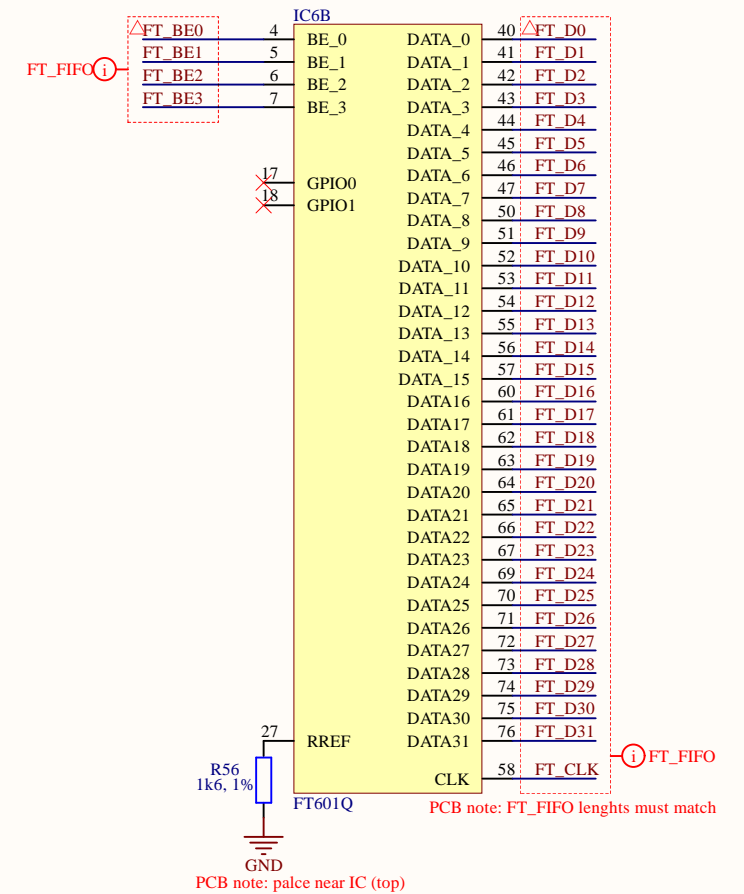
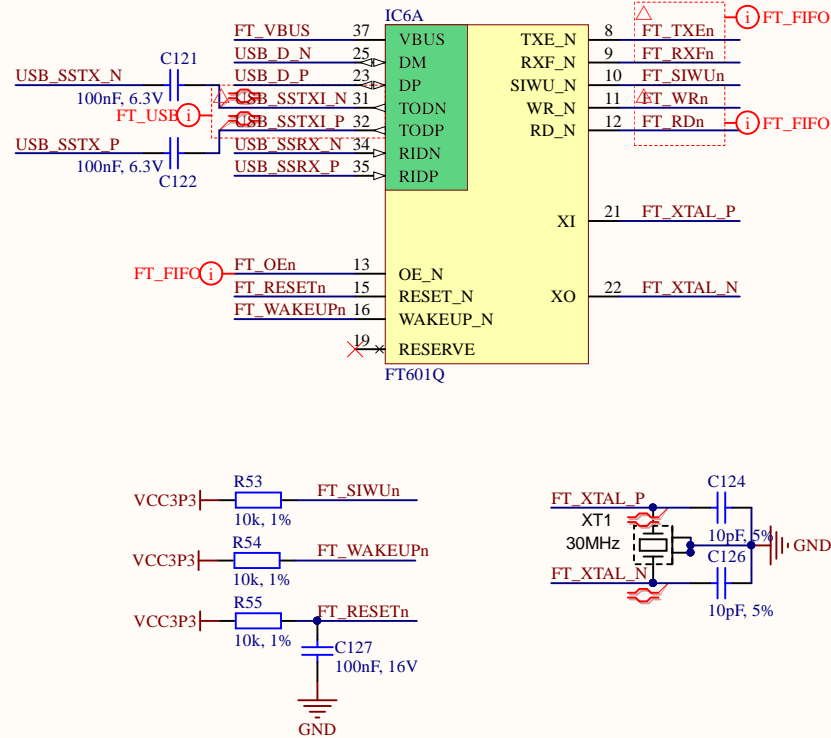
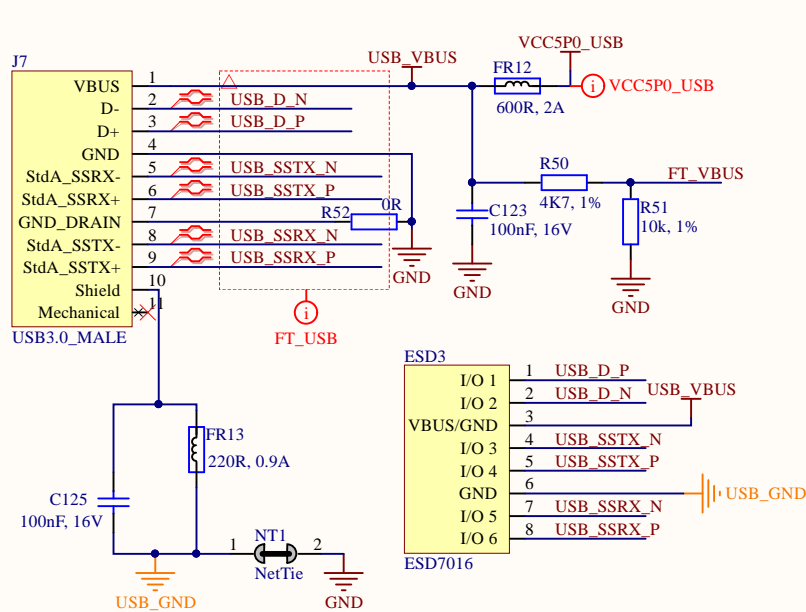
FPGA Power



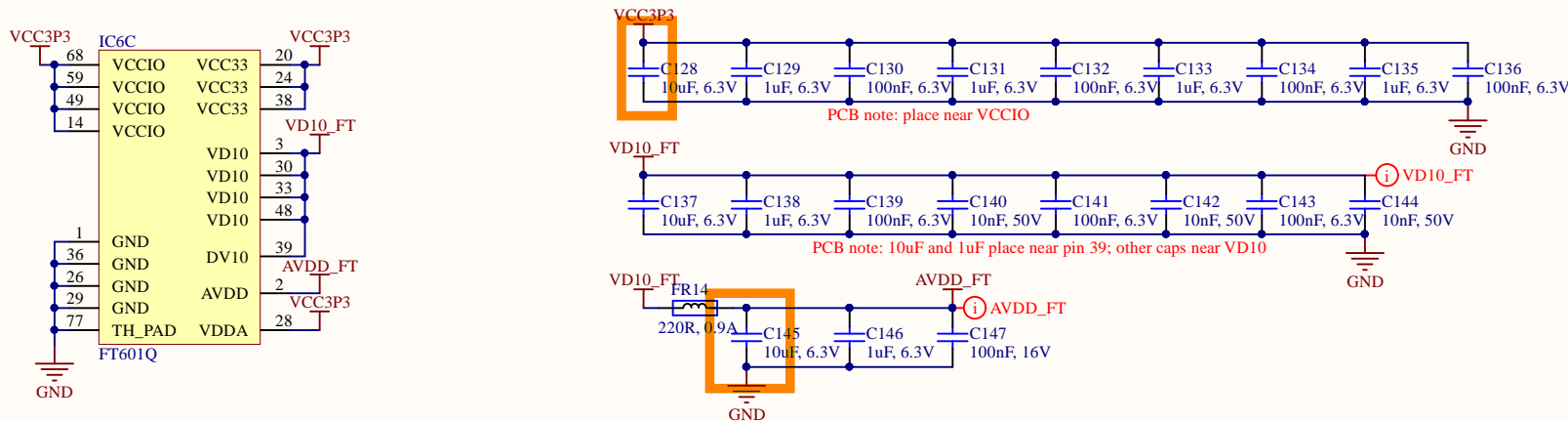
FTDI (USB3) core

USB3.0 plug and

FTDI digital interfaces



FTDI Power



Schematic note: marked 10uF caps not crucial and can be removed to reduce BOM price

Project name: **LimeSDR_Mini_1v1.PrjPcb**

Title: **USB3.0 device**

Size: A3

Revision: v1.1

Date: 2017-12-11

Time: 17:51:20

Sheet8 of 9

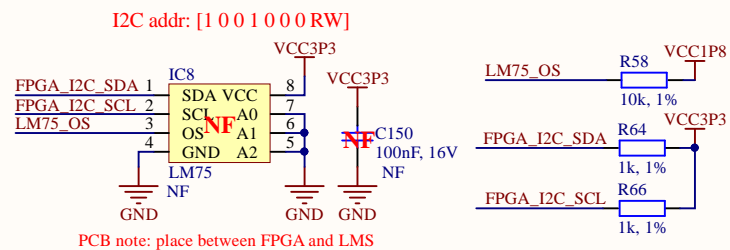
File: 08_USB3_0_device.SchDoc

Lime Microsystems
 Surrey Tech Centre
 Guildford GU2 7YG
 Surrey
 United Kingdom

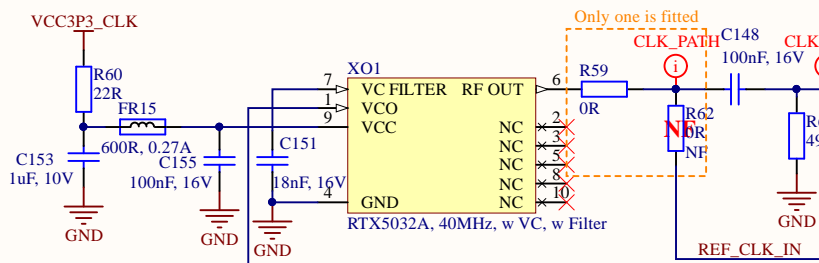


Misc

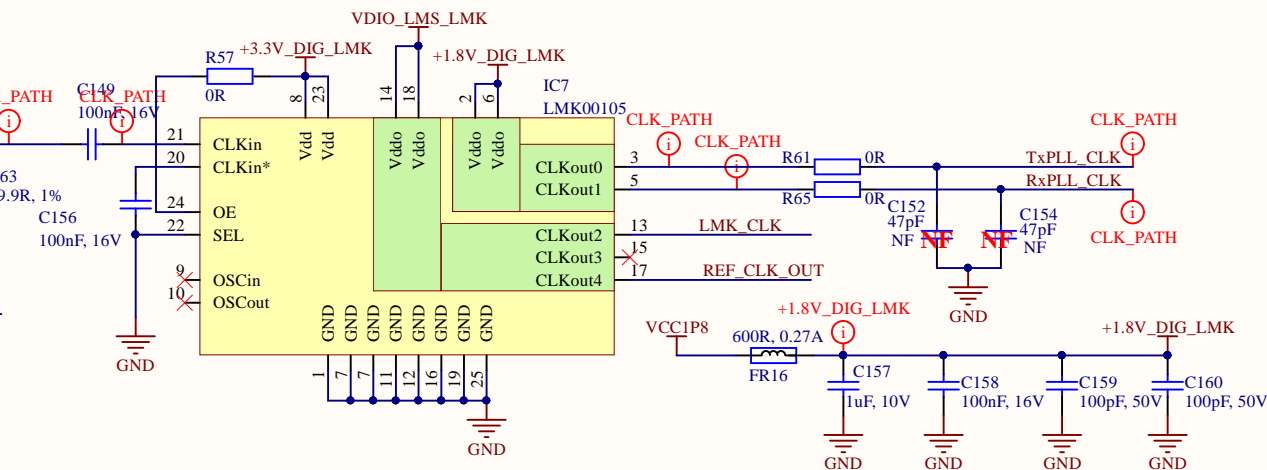
I2C Temperature sensor



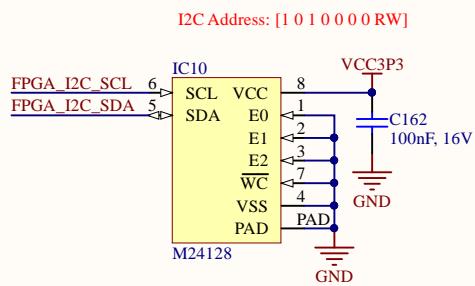
(VC)TCXO



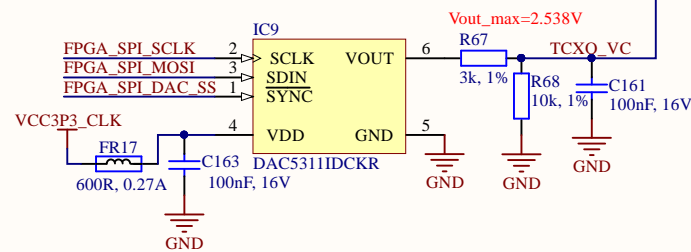
Clock buffer



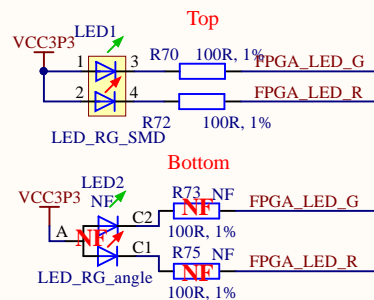
I2C EEPROM



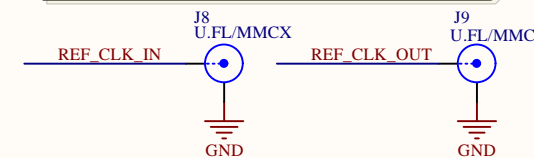
XO DAC



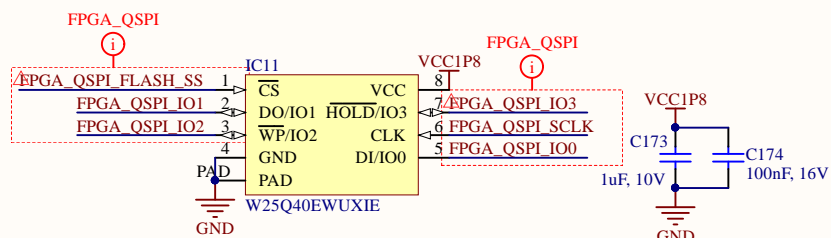
LED (Red/Green)



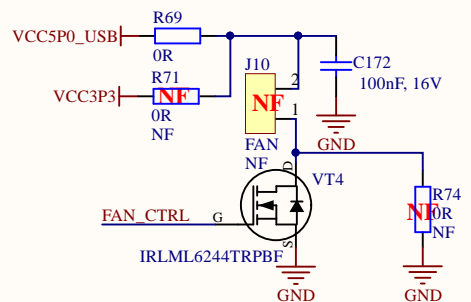
Ref CLK



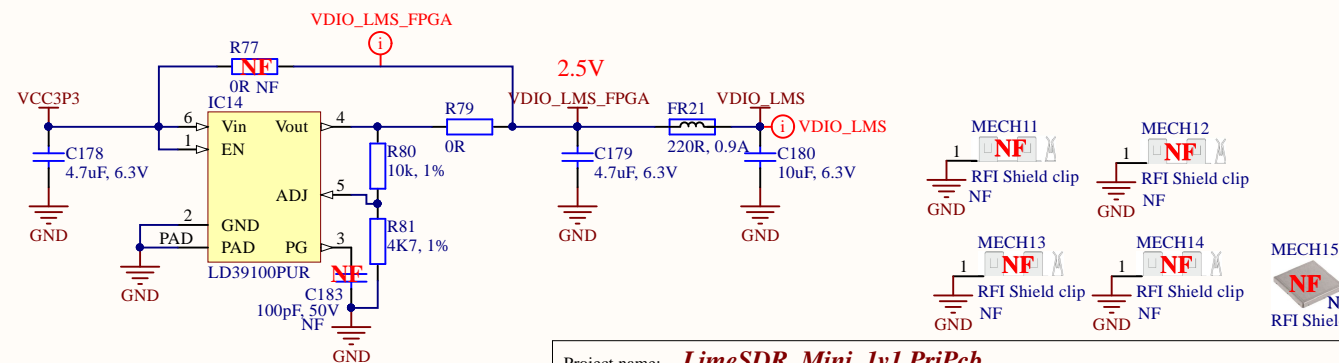
FPGA FLASH



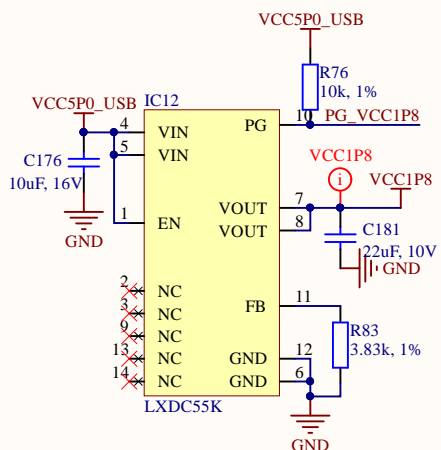
FAN control



Linear regulator (VDIO_LMS_FPGA)



Switching regulator (1.8V)



Switching regulator (3.3V)

