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A Commercial 65 nm CMOS Technology for Space Applications: Heavy Ion, Proton and Gamma Test Results and Modeling

Philippe Roche, Gilles Gasiot, Slawosz Uznanski, Jean-Marc Daveau, Josep Torras-Flaquer, Sylvain Clerc, and Reno Harboe-Sørensen

Abstract—**This paper presents new experimental and modeling evidences that advanced commercial CMOS technologies get intrinsically harder against space radiations with technology downscaling. A 65 nm commercial bulk CMOS process can deliver improved radiation-tolerance without sacrificing electrical performance.**

Index Terms—**CMOS, electronic circuits, radiation hardening, space technology.**

I. Introduction

Scaling introduces new technical considerations and challenges for radiation effects as already described in various tutorials [1]–[3]. For instance, the probability that one particle upsets more than a single SRAM cell increases dramatically for sub-130 nm CMOS technologies, which is a potential threat for error correcting code(s) [4]. However, advanced commercial technologies have been receiving growing attention over the past few years for specific radiation tolerant (rad-tol) and hardened (rad-hard) applications. The main motivation is first the moderate cost of mainstream technologies, compared to specific rad-hard products. Second, the performances of rad-hard ICs generally lag two to three generations behind what is commercially available, accompanied by slower speeds, larger power consumption, and less functionality. Third, tremendous efforts have been made by major semiconductor companies over the past decade to tackle the soft error rate (SER) issue, also driven by the harsh reliability constraints of automotive applications. The improvements made for the terrestrial environment have direct positive consequences for single event effects (SEE) in space, and also for medical applications [5]–[7]. Fig. 1 illustrates what are the predominant radiation effects in the terrestrial [3], medical [8], and space [9] radiation environments.

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Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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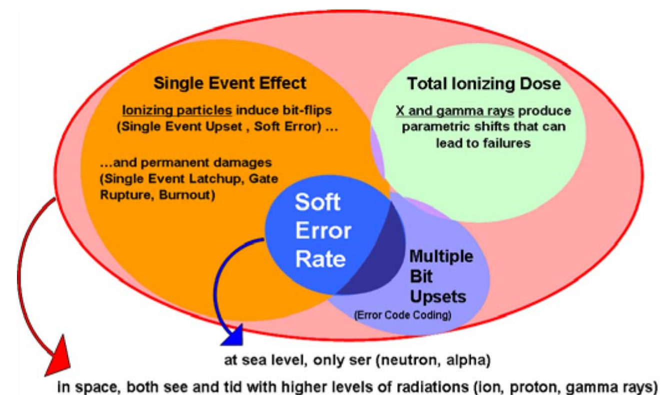

Fig. 1. Radiation failure modes adapted from [3].

In this work, we explore through testing and modeling the radiation response of the STMicroelectronics (ST) commercial CMOS 65 nm technology. The single event upset (SEU), single event latchup (SEL) and total ionizing dose (TID) responses of 12 SRAMs and 6 flip-flops from production libraries are characterized with heavy ions, protons and gamma rays. The first section describes the radiation test plan for four complex test vehicles. The second section synthesizes heavy ion and proton test data for the commercial 65 nm SRAMs. The impact of high temperatures, 125 °C, is quantified as well as the maximum supply voltage, here 1.44 V. The heavy ion SEU cross-sections are also compared for 5 consecutive generations of ST SRAMs from 250 to 65 nm. Furthermore, a comparative analysis between proton and white neutron data is performed using the 65 nm circuits. The third section presents protons and heavy ions test data for representative flip-flops from 65 nm production libraries. The fourth section is devoted to modeling aspects. SPICE simulations, 3-D TCAD simulations and a propriatary Monte Carlo simulator are used to investigate the strong influence of the test pattern, diffusion-collection process, high temperature and supply voltage on SEU rates. The fifth section demonstrates that SRAMs processed in ST 65 nm CMOS are TID immune to 100 krad(Si). Finally, the last section presents the original SRAMs mixed with Hardened by Design (HBD) and Process (HBP) concepts. They take advantage of both the electrical performances and intrinsic TID immunity, which naturally come with commercial deep submicron processes, together with a strong SEU hardness obtained from an original ST mitigation technique applied at design level.

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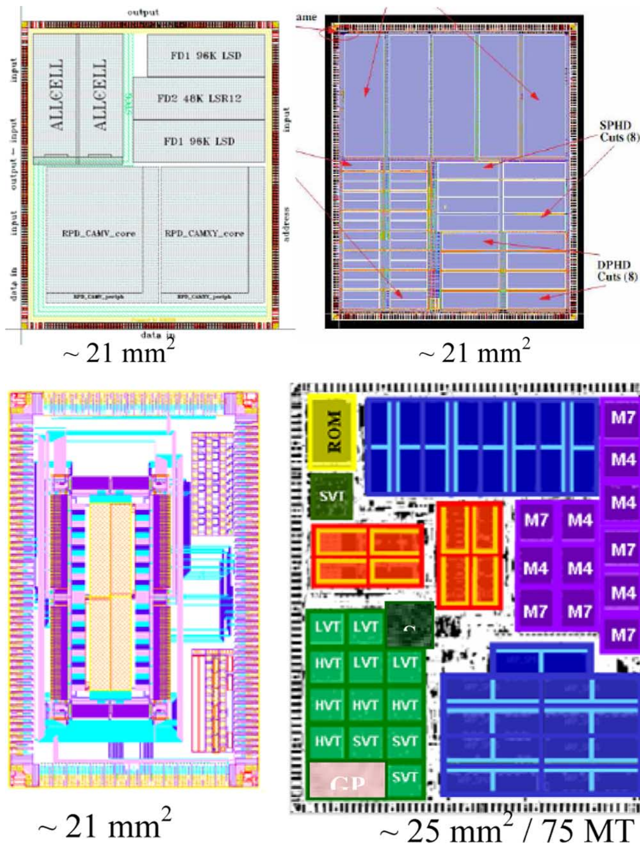

Fig. 2. Floor plans of the four test vehicles designed and manufactured in a 65 nm CMOS technology and then tested at ground level with space radiations.

II. Tested Circuits in 65 nm and Test Plan

Four testchips were designed and manufactured in the ST CMOS 65 nm technology. Fig. 2 illustrates circuit complexities.

The test vehicles embed both SRAMs and flip-flops, as well as representative standard devices from ST production libraries. They were originally designed for SER characterizations of standard production libraries, validation of rad-hard high density (HD) SRAMs and for library validation and qualification, as well as PROcess MOnitoring in the time (PROMO in short, periodically manufactured and tested for months). This latter chip contains SRAMs, ROMs, standard cells, via chains (for back-end stress), ring oscillators (for speed measurements), dividers (for delay path measurements), IOs, fuses, and other devices, for a total of 75 M (million) transistors.

Overall, 46.5 Mbits of SRAMs and ~1 M flip-flops were dynamically measured at ground level under space radiations. The SEE and TID responses of the following design parameters were determined:

- 4 SRAM areas: 0.52 μm^2, 0.62 μm^2, 0.67 μm^2, 0.98 μm^2 SRAM architectures: SP (single port) and DP (dual port);
- two technologies: commercial BULK and SOI 65 nm (SOI test data on similar SRAMs are beyond the scope of this paper);
- one standard process option to remove latchup: the Deep N-Well (DNW) buried layer [4];
- two threshold voltages: standard and high VT (for ultra low power);
- one SRAM covered by two eDRAM capacitors (specifically hardened against atmospheric neutrons);
- six flip-flop (FF) types from production libraries selected for their key SEU features: density, drive, usage of Deep-N Well [4] and architecture. The list of FFs is given in Table II.

Four test campaigns, one week long each, were carried out at RADEF, UCL, ESTEC and PIF test facilities recommended by ESA (https://escies.org/), from the end of 2006 to mid-2007.

A comprehensive Design-of-Experiment was carried out with the following test parameters: pattern (physical checkerboard, Solid 0 and 1), power supply (nominal, plus and minus 20%), temperature (27 °C, 85 °C, and 125 °C), test algorithms (static and also dynamic for accurate Multiple Cell Upset counting), batch-to-batch variations (two to four samples tested per circuit with one spare in case of discrepancy), 16 different ion-LETs, four proton energies, and current monitoring every second on every power line during TID measurements up to 100 krad(Si) (maximum dose used during testings).

Overall, 593 test runs were performed during seven months.

III. SEE Test Results on Commercial SRAMs

A. Heavy Ion Test Results for SRAMs

Fig. 3 shows the experimental heavy ion SEU cross-sections of 6 standard eSRAMs, not protected by any particular mitigation technique, manufactured in commercial ST CMOS 250, 180, 90, 65 nm technology nodes. The error cross-sections are plotted as a function of the linear energy transfer (LET). Tests were carried out at different radiation facilities across Europe (France, Belgium, Finland) and in the U.S. (Brookhaven National Labs), in compliance with the ESA test standard n°22900 [10]. Whereas all LET threshold values remain in the same zone, below 5 MeV.cm^2/mg, the asymptotic cross-sections get smaller with the technology shrinkage, i.e., the intrinsic robustness improves naturally and significantly. All cross-sections are lower than 1E-7 cm^2/bit below CMOS 130 nm, down to 1E-9 cm^2/bit which is low susceptibility when keeping in mind that no mitigation technique was used. The 65 nm SRAM with DNW exhibits a higher sensitivity in comparison to that in 90 nm. This is due to a stronger multiple cell upset (MCU) component with DNW [4]. Whatever the amount and magnitude of MCU, no multiple bit upset (MBU) was ever recorded due to the natural bit interleaving in the tested memory arrays [4]. As a recall, MCU is physical adjacency and MBU is logical adjacency (in the same word). Furthermore, no hard fails were detected during the tests, even with LET 120 MeV.cm^2/mg. Last, but not least, no latchup event was ever measured, even in extreme test conditions for the power supply (nominal +40%), temperature (125 °C) and LET 120 MeV.cm^2/mg, corresponding to Xenon at 1.2 GeV, with a 97 μm range, 60° tilt and 0° and 90° roll angles. More details about the heavy ion test results in 250, 130, and 90 nm can be found in [11].

It is noteworthy that SEU cross-sections at saturation have intrinsically been reduced by 30 × from the 250 nm to 65 nm

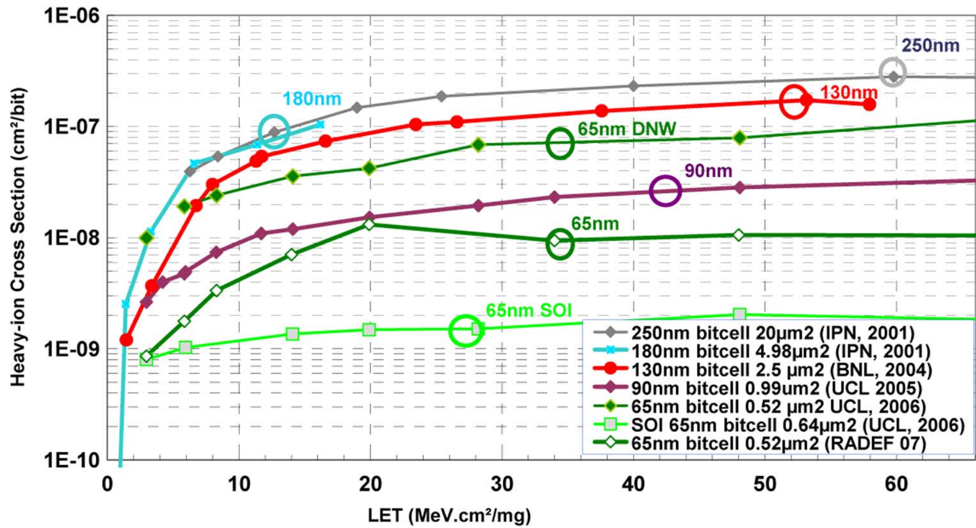

Fig. 3. Heavy ion cross-sections for six commercial SRAMs in standard CMOS technologies. IPN stands for Institut de Physique Nucléaire, Paris; UCL for Université Catholique de Louvain-La-Neuve, Belgium; RADEF is at Jyväskylä, Finland.

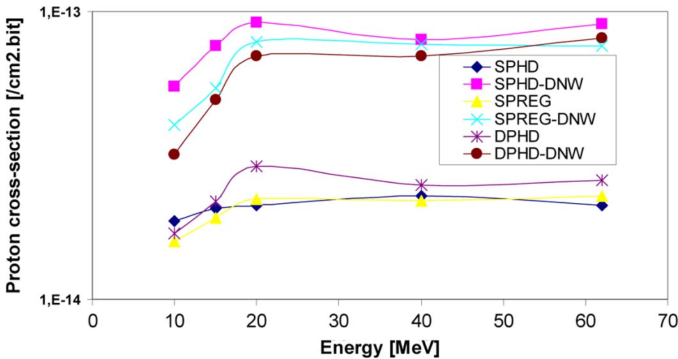

Fig. 4. Proton SEU cross-section carried out at PSI proton test facility, Switzerland, for six standard SRAMs in ST commercial 65 nm CMOS technology. Tests performed in 2007 with a proton beam line limited to 62 MeV.

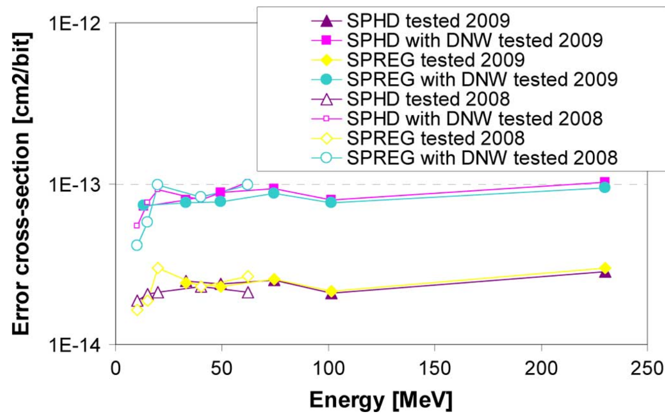

Fig. 5. Proton SEU cross-section carried at PSI proton test facility, Switzerland, for six standard SRAMs in ST 65 nm CMOS technology. Superimposition is made for two set of proton data collected in 2007 and 2009 on two PSI beam lines, respectively limited to 62 MeV then 230 MeV.

technology nodes. As a consequence, moving from the 250 nm technology to 65 nm naturally improves by 60 $\times$ the heavy ion SEU rate/bit/day. This ratio has been estimated with CREME96 calculations for a GEO orbit, minimum solar activity and 100 mils Aluminum shielding. Sensitive areas were calculated as the square root of the asymptotic cross-sections. The sensitive depths were chosen twice deeper for 250 nm than for 65 nm (2 μm).

B. Proton Test Results for SRAMs

Fig. 4 shows the proton cross-sections for six commercial SRAMs in CMOS 65 nm, single and dual port types, covered or not by Deep NWell [4].

All proton cross-sections are flat down to 20 MeV, with decreasing cross-sections at the lowest energies. 10 MeV was the smallest energy available during this experiment (primary beam at 63 MeV). No increase of the cross section is observed near 10 MeV with those BULK 65 nm SRAMs contrary to what we measured for our SOI 65 nm SRAMs tested in the same conditions [11]. This susceptibility of the SOI 65 nm to low energy protons was more pronounced during specific tests with the thick package lids, made of steel, intentionally introduce to further degrade the incident 10 MeV energy down to few MeV. Again, the BULK 65 nm SRAMs did not exhibit such a sensitivity inversion in the same test configuration with the lids. This suggests that our BULK 65 nm technology is not susceptible to direct proton ionization, contrary to the SOI 65 nm counterpart (having similar critical charges but negatively counter-balanced by bipolar amplification). Further investigations and tests will be required around 1–3 MeV.

The overall cross-sections range from 1E-14 to 1E-13 cm^2/bit. The cell area (here 0.52/0.62/0.98 μm^2) does not significantly influence the asymptotic cross-sections, at least according to this first set of measurements limited to 62 MeV. The choice of 62 MeV as the maximum energy was driven by some logistical constraints with the PSI beam line in the 2008 timescale. In order to investigate any deviation of the asymptotic cross section at higher energies, a second set of measurements was performed up to 230 MeV in July 2009. A new PSI beamline was used with discrete proton energies

TABLE I
INCREASE OF SEU CROSS-SECTIONS AT HIGH TEMPERATURE MEASURED ON ST 65 nm SRAMS

	Highest temperature used for the heavy ion testings	Cross-section increase at saturation between room and highest temperature
Chip A: SRAM #1 and #2	**+85 °C**	**+37%** and **+42%**
Chip B: SRAM #1 and #2	**+125 °C**	**+30%** and **+42%**
Chip C: SRAM #1 to #6	**+125 °C**	**+52%** on average

TABLE II
LIST OF RADIATION TESTED FLIP-FLOP FROM ST 65 nm PRODUCTION LIBRARIES

	Flip-flops selected for radiation testings	FIFO size	DNW
FFA	Plain-FF, lowest drive	199 K	yes
FFB	Plain-FF, highest drive	160 K	yes
FFC	Plain-FF, highest drive, HD	194 K	yes
FFD	Clear-FF, lowest drive	133 K	yes
FFE	Plain-FF, lowest drive, HD	194 K	no

ranging from 10 to 230 MeV. Fig. 5 shows the very good agreement between the two PSI beamlines.

During 2009 testings, four samples were tested with a proton fluence for each energy set to 2E10 p/cm^2. With a 60% confidence limit and chi square statistical model, the magnitudes for the lower and upper limits for all proton cross-sections respectively range from 3E-17 to 3E-16 and 2E-16 to 1E-15 cm^{-2}.bit. Those error bounds are not reported for each average cross section in Fig. 5 for sake of clarity. Those small error bars allow to state that the mean proton cross-sections are similar at 62 and 230 MeV. It should be noted that for highly-scaled CMOS, total cross sections (SBU plus MCU) do not saturate due to the increase of MCU at high energies or LETs. Another observation drawn from Fig. 5 is that a decrease in the proton cross section occurs at 100 MeV. This dip, as originally suggested in [12], is related to variations in neutron/proton nuclear interaction cross-sections which have a local minimum at 100 MeV.

The extended proton testings on SRAMs have also confirmed that the DNW process option, used for a full latchup immunity with heavy ions, leads to an increase of the proton cross-sections by 5 $\times$. This gap is again attributed to the higher MCU component with DNW [4], but this is not prejudicial when applying ECC/EDAC since no MBU occurs at 230 MeV. Here again, physical MCU did not transform into logical MBU because of the bit interleaving or bit line scrambling for the tested SRAMs. It is finally noteworthy that neither hard fail, nor latchup was measured at 230 MeV with a cumulative fluence of 9E11 protons/cm^2.

C. SEU Variations at High Temperature and Power Supply

The impact of temperature on the SEU cross section is also quantified in this work. The motivation is the high temperature constraint associated with space (125 °C) but also automotive (150 °C) applications. Our contribution, in this section with heavy ion test results and later on with simulations, lies within the scope of previous studies [13], [14] and more recently by [15]. This latter paper has concluded that no predominant parameter exists and that temperature dependence for SEU results from a complex mix of factors which will be further examined in Section VI.C.

Temperature influence is quantified with heavy ions over ten different SRAMs embedded in three testchips. Test results show that the higher the LET, the stronger the temperature impact is. On average the SEU cross-sections at saturation increase by 30%–50% from 30 °C to 125 °C, as summarized in Table I.

The impact of the power supply voltage has also been assessed with heavy ion testings. A uniform and relatively small shift of the cross-sections was observed across the whole LET range by changing the power supply voltage. The lower the supply voltage is, the higher the cross-sections are, and vice versa. An increase of the VDD by +20% for the tested SRAMs, with and without DNW, leads to +15% and +12% increases on average for the cross-sections at saturation. That is not significant within the experimental uncertainty.

The next Section IV is devoted to modeling and discusses the phenomelogical explanations for cross section increases with both high temperature and power supply.

IV. SEE TEST RESULTS ON COMMERCIAL FLIP-FLOPS

While designing an IC using standard-cell libraries, the choice between large variety of FF and latches has to be made depending on the desired functionality (e.g., scannable or non-scannable; plain-, clear-, or preset-FF), timing properties, drive strength, power dissipation, etc. When moving into the technology nodes beyond 130 nm, the error cross-sections of sequential elements are a new design metric that has to be taken into account. Therefore, a characterization study comparing SEU cross-sections of different FFs from 65 nm standard-cell libraries used in our production design environment is presented here.

As previously indicated, a dedicated test-chip (upper right floor plan in Fig. 2) was designed to measure the radiation susceptibility of five different FFs. The circuit was processed in a 65 nm CMOS process optimized for low-power applications, with a nominal supply voltage set to 1.2 V (1 V by default). The chip contains five first-in, first-out (FIFO) shift registers, containing from 133 K to 199 K identical cells each. A large number of cells are required to obtain accurate SEU data within an acceptable test time. To prevent data corruption due to upsets at clock nodes [16] the entire clock-tree was made single event transient (SET) immune with a proprietary mitigation technique. The test-input and test-enable signals (in the case of scannable FFs) and the clear-data signal (in the case of clear-FFs) were fixed with the use of tie-off cells, to prevent internal nodes from floating.

The FFs were selected from standard-cell libraries that are used in the design of production chips. Because the five FFs are commonly used in production designs, they are well suited for a comparative study of the effect of different design choices on the FF radiation sensitivity in real-life IC designs. The main characteristics of tested FFs are listed in Table II.

Static tests were performed by writing either a Solid1 or Solid0 pattern, or physical checkerboard, into the shift registers. The clock signal (CLK) was set either to a constant high or

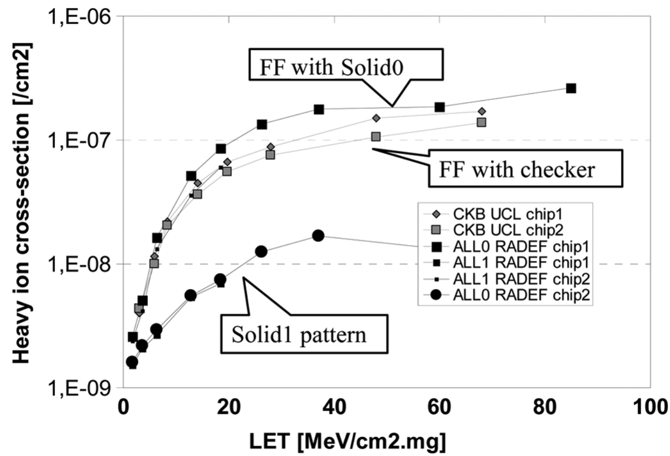

Fig. 6(a). Heavy ion SEU cross-sections carried out at UCL and RADEF heavy ion test facilities for standard flip-flops in ST commercial 65 nm CMOS technology. Static tests with solid and checker patterns at nominal VDD and temperature conditions. FF features are listed in Table II. (b) Proton SEU cross-sections carried out at PSI proton test facility for standard Flip-flops in ST 65 nm. Static tests with solid and checker patterns at nominal VDD and temperature conditions. FF features are listed in Table II.

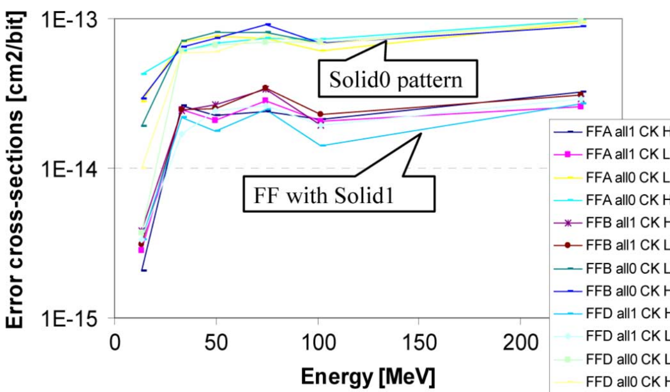

Fig. 6(b). Proton SEU cross-sections carried out at PSI proton test facility for standard Flip-flops in ST 65 nm. Static tests with solid and checker patterns at nominal VDD and temperature conditions. FF features are listed in Table II.

to constant low value during irradiation. The master latch is sensitive to upsets in the CLK $=$ HIGH state, while slave for CLK $=$ LOW (cf. Fig. 9). Thus, error cross section is measured at four different operational conditions, due to the combination of two data and two clock states. In the present work we focus on the cross-sections of FFs under static conditions. Our conclusions also apply up to 12.5 MHz which was the maximum speed during irradiation of those shift registers. For a detailed discussion on the FF sensitivity with dynamic conditions the reader is referred to [17]. Fig. 6 respectively shows the heavy ions and proton test data for the flip-flops in Table II.

All heavy ion and proton SEU cross-sections range over two decades with a moderate influence of the FF type. A comprehensive description of the flip-flops and their responses to both alpha and neutron irradiations are given in [18]. The test pattern is confirmed to have the strongest impact on the SEU susceptibility: Solid 0 pattern gives 10 $\times$ more errors than Solid 1 for each test condition. The next modeling section allows understanding this experimental fact.

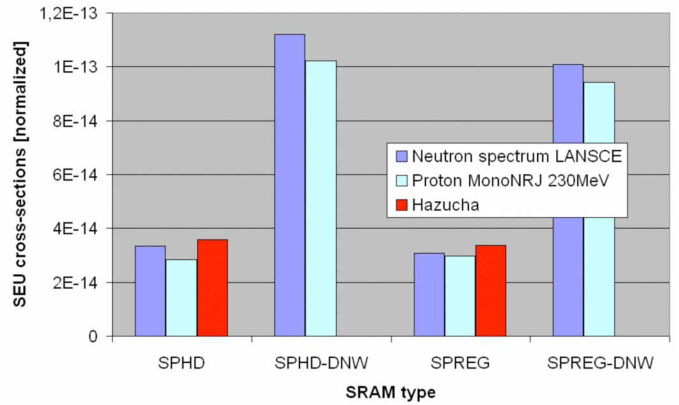

Fig. 7. Comparison between neutron and proton cross sections for SRAMs 65 nm. Analytical modelling calibration is performed from a single SRAM and allows predicting the cross-sections of other SRAM architectures.

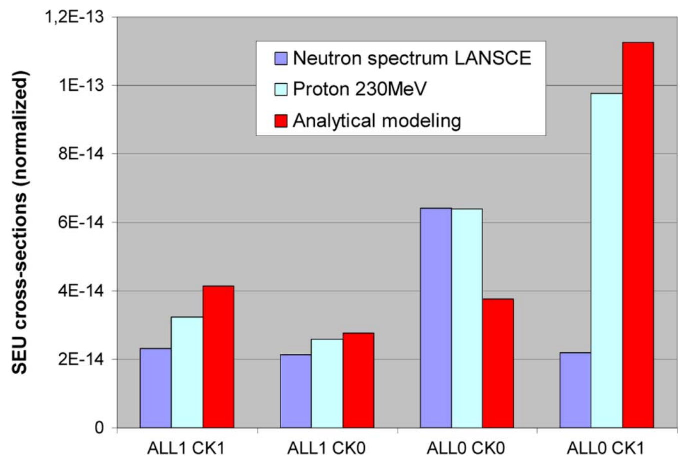

Fig. 8. Comparison between neutron and proton cross sections for a reference FF tested under neutrons and protons. Analytical modelling is performed with η and K parameters extrapolated from neutron tests on a single SRAM.

V. Convergence of Proton and Neutron Sensitivity for 65 nm Memory Devices

Usage of neutron cross-sections for proton predictions and vice-versa has been the quest of many research teams for years [12], [19]. It is commonly admitted that protons and neutrons above 50 MeV have comparable effects in microelectronics devices. Moreover, at energies below 50 MeV the main nuclear effect at play is elastic interaction whose energy deposition is small. The critical charge of a bitcell is important when comparing neutron and proton data. It was shown for a 180 nm SRAM that its sensitivity to neutrons is comparable between 14 MeV and white neutron spectra, with energies ranging from a few to 100's of MeV [12], [19]. For a modern 65 nm SRAM, it can be seen in Fig. 5 that the proton cross section is almost constant over the entire energy range. There is less than a factor of two between the minimum and maximum cross-sections. Fig. 7 further compares SRAM cross-sections measured with 1–800 MeV neutrons at LANSCE and with 230 MeV protons at PSI: they are identical for two different bitcell architectures processed with and without Deep-Nwell. As a practical consequence, neutron test data owned by major semiconductor companies could be conveniently extrapolated to predict device

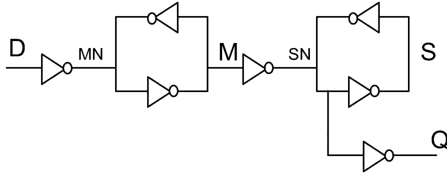

Fig. 9. simplified schematic of the flip-flop. The sensitive nodes are labeled as MN, M, SN and S.

sensitivity to space protons for 65 nm applications and below (provided that the technology is not sensitive to low-energy protons).

Fig. 8 presents cross sections calculated from a well known analytical model [20] whose expression is

$$\text{Error Cross-Section} = K \cdot [\mathrm{A}_{\mathrm{diff,N}} \cdot e^{-\mathrm{Qcrit}_{\mathrm{electron}}/\eta_{\mathrm{electron}}} + \mathrm{A}_{\mathrm{diff,P}} \cdot e^{-\mathrm{Qcrit}_{\mathrm{hole}}/\eta_{\mathrm{hole}}}]$$

where $\mathrm{A}_{\mathrm{diff}}$ is the drain area for sensitive nodes, Qcrit the critical charge, η the collection efficiency parameters, and K depends upon the radiation which is used. η and K are extrapolated from one neutron experimental test result on one single SRAM and then used to model every other SRAM and FF. Fig. 8 shows that experimental neutron and proton cross-sections are both very well fitted by analytical modelling. Hence, once calibrated from a single neutron test, this model allows predicting with a good agreement neutron and proton cross-sections for SRAMs and a raw modelling for FFs (with higher Qcrit, thus more energy dependence).

VI. SEU Modeling for Commercial 65 nm Flip-Flops and SRAMs

A. *SPICE Simulations to Investigate Pattern Effect for FFs*

Fig. 9 shows the typical schematic of a flip-flop composed of two latches. This simplified electrical view aims at illustrating the use of the two (clocked) cross-coupled inverters which also constitute the elementary device of most static RAM architectures.

In retention mode, where the logical information is stored in the master or slave stage, the critical charges (Qcrit) of a flip-flop and an SRAM cell can be compared. Qcrit is defined as the minimum charge which has be collected at a given electrode to induce an upset. Table III shows such a comparison for a regular SRAM cell and the multiple sensitive nodes of basic flip-flops (see the corresponding node labels in Fig. 9). SPICE simulations were run for the 65 nm CMOS technology and typical conditions at 1.2 V.

The link between the computed critical charges and related electrical nodes inside FFs are explained in details in [18].

Results in Table III show that the critical charges are higher when the master or slave stores a '0' state. Besides, master M and MN nodes involve more diffusion areas (1.2–1.3× larger) when latching a '0' than with '1'. It is about the same proportion for slave S and SN. According to Hazucha formula [20] both lower critical charges and larger diffusion areas explain why the SEU cross-sections are 10× higher with a solid '0' test pattern compared to '1', as experimentally reported in Figs. 6–8.

TABLE III
Critical Charges for the Flip-Flops and Regular SRAM Cells in 65 nm CMOS Technology

Qcrit in fC nominal conditions	Data = 1				Data = 0			
	Clock = 1		Clock = 0		Clock = 1		Clock = 0	
	Master M	MasterMN	Slave SN	Slave S	Master M	MasterMN	Slave SN	Slave S
FF A	60,0	2,8	10,9	3,2	3,1	4,3	50,0	3,2
FF B	27,9	2,8	infinite	8,9	4,3	3,1	infinite	8,9
FF C	5,0	2,3	521,3	2,7	4,2	2,5	infinite	2,8
FF D	5,0	3,5	infinite	3,5	4,0	4,0	4,3	3,8
FF E	5,0	2,3	521,3	2,7	4,2	2,5	infinite	2,8
DPHD	1,85				1,59			
SPREG	1,53				1,59			
SPHD	1,47				1,50			

Table III also compares the Qcrit of flip-flops and SRAM cells, for the single port (SP) and dual port (DP) architectures, high density (HD) and single register (REG) design features. For the most sensitive nodes, the Qcrit for the flip-flops has the same order of magnitude as for the SRAM cells. On average it is higher for FFs due to both the larger sizing of the transistors and higher inverter strengths. These latter differ from the master to the slave stage. For the 65 nm CMOS technology, the similar critical charges and diffusion areas lead to the same order of magnitude for SRAM and flip-flops SEU cross-sections reported in Figs. 3, 5, and 6. It is recalled here that logic parts of modern circuits bring the highest SEU rate once the memories have been protected by EDAC. A few major semiconductor companies are presently offering new radiation-hardened FF libraries, as an alternative to the costly triple modular redundancy technique (multiple identical logic paths feeding into a majority voting).

B. *3-D TCAD Simulations to Calculate Diffusion-Collection Coefficients Within a Realistic Flip-Flop*

Fig. 10 shows the 24 adjacent transistors of a 65 nm flip-flop, labelled FFA in Table II, entirely modeled in a 3-D contiguous TCAD domain using a specific flow adjusted from SENTAURUS tool suite. From this outstandingly complex structure were extracted both the ambipolar diffusion and collection velocity coefficients used in the Monte Carlo code presented in the next section. The main motivation was to verify that those D* and v* parameters [21] can be determined with the same accuracy (at ±5%) using either a realistic complex FF or simplified 3-D pMOS and nMOS TCAD devices.

The CPU time benefit is very high, in the range of 1 to 2 days for the elementary MOS devices against a few weeks for the complete FF, using state-of-art OPTERON multi-core processors.

C. *Proprietary Monte Carlo Simulations to Investigate High Temperature and Power Supply Effects on SRAMs*

A Monte Carlo SEU simulator is run to reproduce the experimental heavy ion SEU cross-sections for the ion cocktail available at RADEF. The ion-induced current is computed using the diffusion-collection model extensively presented in [21]–[24]. The key input parameters for this model, i.e., the ambipolar diffusion coefficient and the collection velocity, were calculated

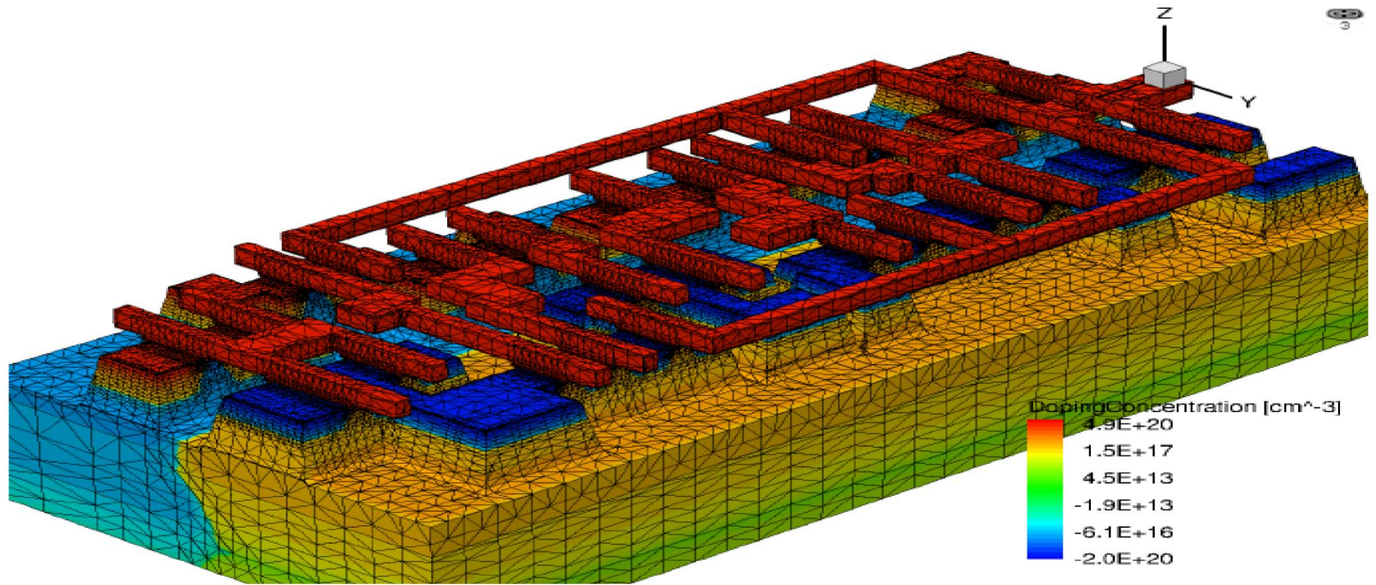

Fig. 10. 3-D TCAD modeling of the flip-flop FFA in Table I. Shallow Trench Isolations made of SiO^2 are removed from this display for clearness reasons.

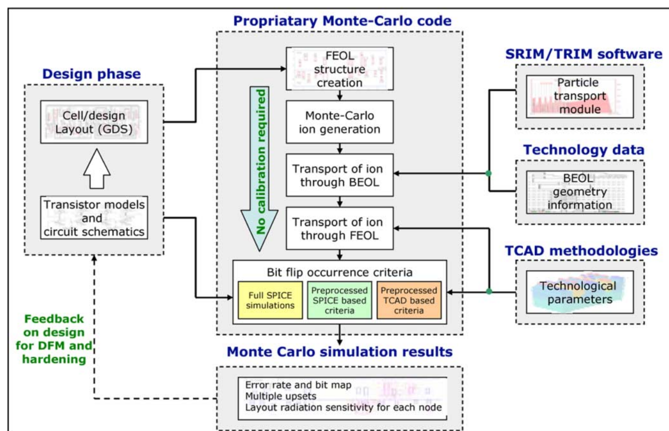

Fig. 11. Flow for our radiation Monte Carlo simulator [25].

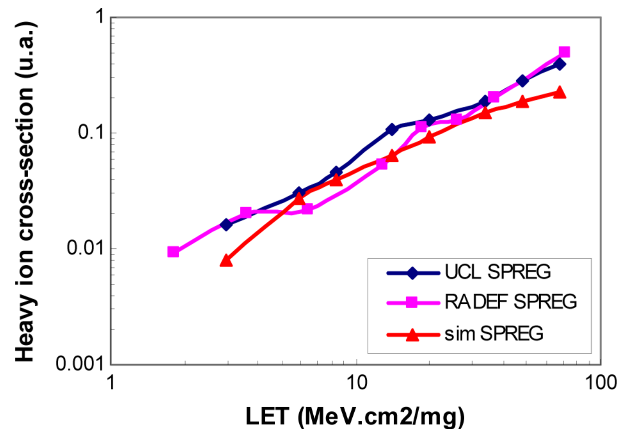

Fig. 12. Agreement between simulations and experimental SEU cross-sections for a commercial 65 nm CMOS SRAM.

for the ST CMOS 65 nm technology node using 3-D TCAD device simulations. The simulation flow is depicted in Fig. 11. All details about the methodology and input parameters are given in [25].

Fig. 12 shows the good agreement found for medium LETs between the simulations and test results for a commercial SRAM without DNW in CMOS 65 nm. For high LET values a slight underestimation of the cross-sections is observed. It is attributed to the parasitic bipolar amplification which is not yet accurately modeled in our simulator. Conclusions can not be drawn at very low LET because of the experimental uncertainty.

The simulator is now used to identify what are the key parameters responsible for the SEU increase at high temperature, experimentally evaluated in the range of +30% to +50% (cf. Table I). It has been reported in [15] that the temperature may impact the error rates by altering the following:

a) the characteristics of the memory cells, in terms of write speed and strength for the restoring device;

b) the current pulse generated by the impinging particles affecting the transport properties of the charge generated by ionizing particles.

Both hypotheses are assessed with new specific Monte Carlo simulations. The input parameters are modified by a) adjusting the temperature parameter to 125 °C in the SPICE netlist and then b) recalculating the technological parameters at 125 °C. Using the semiconductor equations expressed in [26], the ambipolar diffusion coefficients for nMOS and pMOS transistors increase by +9.9% and +17.1% compared to 30 °C. Concurrently, the N and P collection velocities are increased from 30 °C to 125 °C by +5%, in the same proportion as the depletion region width [15]. The Monte Carlo simulations are performed at 30 °C and 125 °C, for the nominal power supply, a solid 1 test pattern and an LET 68 MeV.cm^2/mg, as the lightest LET where the Monte Carlo model give reasonable agreement. The change in the characteristics of the memory cells (SPICE netlist) lead to +21% for the simulated cross-section. The additional

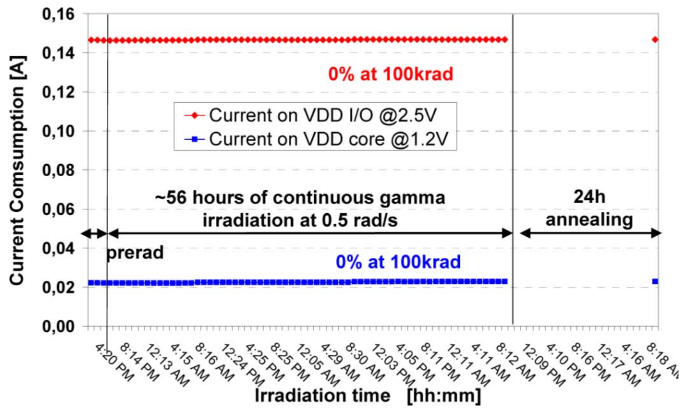

Fig. 13. Leakage currents as a function of cumulated dose for a 4 Mb SRAM in ST commercial 65 nm CMOS technology.

adjustment of the technological parameters (D* and v* parameters) further gives an additional +4%. The total increase of +25% is not in agreement with the experimental increase reported in Table I. The discrepancy, in the range +10% to 25%, is attributed to the bipolar amplification which is maximized at high temperature and for our tested SRAMs which specifically use Deep-NWell [4]. Future work will be required, it has been started in [25], to better account for the parasitic bipolar effect in our simulation environment.

VII. TID Results on Commercial 65 nm SRAM

The TID-induced threshold voltage (Vth) shift [1] in MOSFETs is one of the two major causes of leakage current with gamma and X-rays, with the inversion of the channel under the gate-STI overlap. TID-induced Vth primarily depends on the gate oxide thickness. When the gate oxide becomes thinner than 5 nm the tunneling effect allows for a natural and optimum TID recovery [1]. Various publications have already experimentally confirmed the positive trend towards smaller Vth shifts and lower leakage currents within and in-between devices. Fig. 13 further demonstrates the improvement of the intrinsic TID robustness as the technology feature sizes scale down.

A commercial ST 4 Mb eSRAM in CMOS 65 nm is irradiated by a Cobalt 60 source at ESA-ESTEC premises, for 72 hours until reaching 100 KradSi. The dose rate is set to 0.5 RadSi/s. The test procedure is compliant with the ESA test standard for TID measurements, specifications n °25100 [27]. The current consumption is continuously monitored for both the SRAM core and I/O power supplies, respectively set to 1.2 V and 2.5 V.

The main and obvious conclusion for those TID testings, carried out on four different samples from two lots, is that no change in leakage current occurs. The SRAM is fully immune to TID at the maximum cumulated dose, here set to 100 kradSi.

VIII. SRAMs Hardened With eDRAM Capacitors in Deep Submicron Commercial Technologies

This section illustrates novel design techniques applied to the hardening of a commercial CMOS process. This approach is often referred as Hardness-by-Design (HBD) [1].

A six-transistor (6T) memory cell, with the addition of two stacked capacitors (between polysilicon and metal 1 layer) within the cell footprint, is used in CMOS 130 nm [28], [29] and 65 nm in order to improve the SEU hardness, in conjunction with the strong intrinsic TID hardness.

The memory cell is made of a symmetrical addition of two stacked capacitors, with up to twice 80 fF added per cell. The capacitors are inserted in the middle-end-of-line (MEOL) between the transistors and the first level of metallization, and manufactured with a standard embedded DRAM (eDRAM) process flow. Consequently, the minimum amount of charge required to flip the logic state of the cell, called critical charge ($Q = C\times$ V), is increased, leading to much lower SEU rate. The extra leakage induced by two capacitors is limited to an additional 0.5 fA/Unit at 25 °C with the common node biased at VDD/2.

Fig. 15 shows the heavy ion SEU cross-sections experimentally determined for four rad-hard SRAM variants.

It is confirmed that the higher the added capacitor per cell, the lower the SEU cross-sections for the SRAM. Depending on the application, an optimum trade-off between the speed (capacitor value has an impact on the write cycle time), power, and radiation robustness can be achieved. As an application, a standalone SRAM has been designed for Implemented Medical Devices (defibrillators, pacemakers, etc). Outstanding performances were measured for this 8 Mb memory: a static power consumption of 0.6 mA at 37 °C and 1.4 V and a 100 000× improvement for the neutron and alpha SER. All details can be found in [30].

IX. Conclusion

The SEE and TID failure modes have different magnitudes on a given circuit in the terrestrial, space and medical environments. The terrestrial one brings the softest constraints and space the harshest. In this paper, the relative SEE susceptibility of 5 generations of commercial SRAMs was first experimentally assessed with heavy ions and protons on 65 nm SRAMs and flip-flops from production libraries. A total of 46.5 Mbits and 1 million Flip-flops were characterized under space radiations at ground level. Numerous test and design parameters were taken into account in the test plan, including the test pattern, high temperature, test algorithm and power supply. Overall 593 test runs were performed over several months. The asymptotic heavy ion and protons SEU cross-sections are improved with the downscaling of the minimum feature size and are of moderate magnitude below 130 nm, below 1E-7 cm^2/bit, without any mitigation. For the ST technologies, moving from the 250 nm node to the 65 nm one naturally improves by 60× the heavy ion SEU rate/bit/day for a geostationary orbit. This intrinsic SEU gain assumes that the tested technology is not sensitive to very low LET, below 1.44 MeV.cm^2/mg (lowest experimental LET used for the ST bulk 65 nm), which has not yet been formally verified. Moreover, this SEU benefit is expressed per Mbit and might be minored at chip level due the growing amount of embedded memories when technologies scale down. The proton SEU cross-sections are also low in 65 nm, below 1E-13 bit/cm^2, and almost constant with energy above 20 MeV. As a result, they can be accurately predicted from white neutron testings

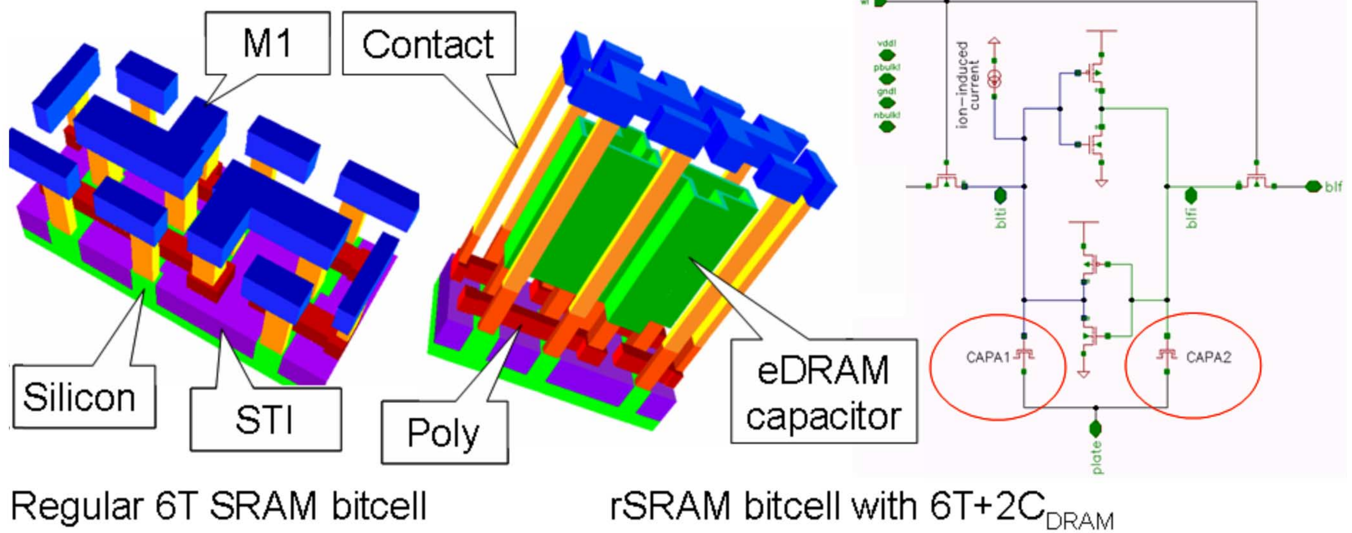

Fig. 14. 3-D views and schematic for a robust SRAM cell composed of six standard transistors plus two eDRAM capacitors $(6\mathrm{T}+2\mathrm{C})$ [27].

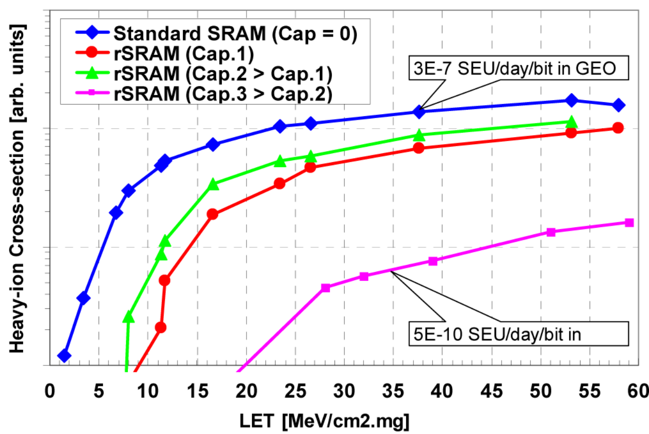

Fig. 15. Heavy ion test results for 4 SRAMs hardened against atmospheric neutrons in 130 nm and 65 nm commercial technologies. Four different eDRAM capacitor values are added on top of elementary SRAM cells. SEU rates are calculated using CREME96, for GEO orbit, worst week, and 100mils Al shieling.

or extrapolated with an analytical model once calibrated with a single neutron test. The related demonstration in the paper assumes that the tested ST 65 nm bulk technology is not sensitive to low energy protons (<3 MeV). This condition is positively supported by our preliminary experimental checkings (cf. III-B) but not yet fully verified.

With the Deep N-Well (DNW) process option, here specific to the semiconductor manufacturer ST, all parts were found to be fully SEL and SEGR free, even with the worst case combination of 125 °C, VDD + 40% and LET 120 MeV.cm^2/mg. Furthermore, the SEU susceptibility of 65 nm flip-flops was measured with heavy ions and protons and found be similar to that of SRAMs. The worst case test condition was observed with the solid 0 pattern. The underlying upset mechanisms were investigated with critical charge SPICE simulations. 3-D TCAD simulations and a propriatary Monte Carlo simulator were also used to quantify the strong influence of the high temperature and supply voltage on SEU rates. The impact of the parasitic bipolar transistor was again confirmed to be significant for such highly integrated devices.

The TID susceptibility is known to become acceptable for gate oxide thicknesses below 5 nm, i.e., below the 130 nm CMOS technology. Several commercial 65 nm CMOS SRAMs were tested with a Cobalt 60. Their full TID immunity was verified at the maximum cumulated dose, here set to 100 kradSi, for both the thin and thick gate oxides used within memory cells and I/O analog parts. Such TID performances demonstrate that a commercial 65 nm CMOS technology can be leveraged for space applications, without having to recourse to costly guard rings or edgeless transistors, or specialized foundries.

Finally, SRAM cells hardened by two eDRAM capacitors were used to improve the SEU hardness, in conjunction with the strong intrinsic TID hardness. Heavy ion testings confirmed that the higher the added capacitor per cell, the lower the SEU cross-sections are. An example of optimum trade-off between power and radiation hardness was presented. Using an innovative (in 65 nm) RHBD technique, electrical performances and radiation-hardness can be both met in advanced commercial CMOS technologies.

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