RF Agile Transceiver

AD9363

FEATURES

- Radio frequency (RF) 2 × 2 transceiver with integrated 12-bit DACs and ADCs
- Wide bandwidth: 325 MHz to 3.8 GHz
- Supports time division duplex (TDD) and frequency division duplex (FDD) operation
- Tunable channel bandwidth (BW): up to 20 MHz
- Receivers: 6 differential or 12 single-ended inputs
- Superior receiver sensitivity with a noise figure: 3 dB
- Receive (Rx) gain control
  - Real-time monitor and control signals for manual gain
  - Independent automatic gain control (AGC)
- Dual transmitters: 4 differential outputs
- Highly linear broadband transmitter
  - Transmit (Tx) error vector magnitude (EVM): −34 dB
  - Tx noise: ≤−157 dBm/Hz noise floor
  - Tx monitor: 66 dB dynamic range with 1 dB accuracy
- Integrated fractional N synthesizers
  - 2.4 Hz local oscillator (LO) step size
- CMOS/LVDS digital interface

APPLICATIONS

- 3G enterprise femtocell base stations
- 4G femtocell base stations
- Wireless video transmission

FUNCTIONAL BLOCK DIAGRAM

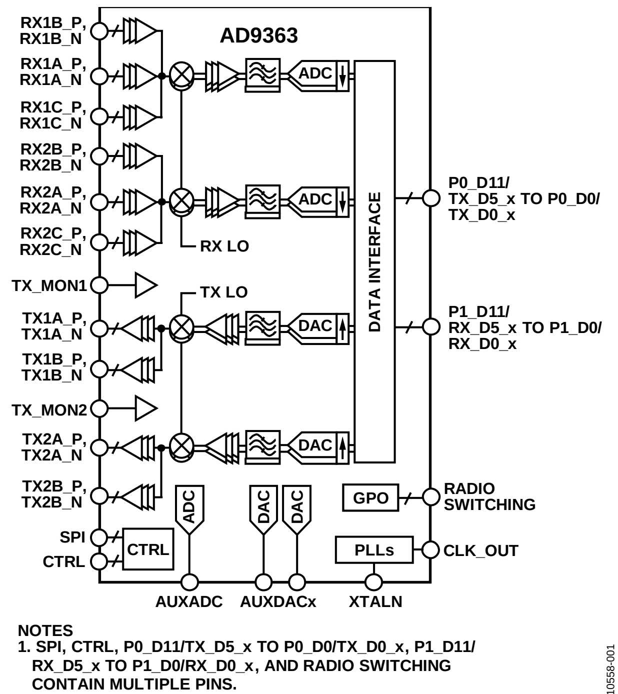

Figure 1.

GENERAL DESCRIPTION

The AD9363 is a high performance, highly integrated RF agile transceiver designed for use in 3G and 4G femtocell applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The AD9363 operates in the 325 MHz to 3.8 GHz range, covering most licensed and unlicensed bands. Channel bandwidths from less than 200 kHz to 20 MHz are supported.

The two independent direct conversion receivers have state-of-the-art noise figure and linearity. Each Rx subsystem includes independent automatic gain control (AGC), dc offset correction, quadrature correction, and digital filtering, thereby eliminating the need for these functions in the digital baseband. The AD9363 also has flexible manual gain modes that can be externally controlled. Two high dynamic range ADCs per channel digitize the received I and Q signals and pass them through configurable decimation filters and 128-tap finite impulse response (FIR) filters to produce a 12-bit output signal at the appropriate sample rate.

The transmitters use a direct conversion architecture that achieves high modulation accuracy with ultralow noise. This transmitter design produces a best-in-class Tx EVM of −34 dB, allowing significant system margin for the external power amplifier (PA) selection. The on-board Tx power monitor can be used as a power detector, enabling highly accurate Tx power measurements.

The fully integrated phase-locked loops (PLLs) provide low power fractional N frequency synthesis for all receive and transmit channels. Channel isolation, demanded by FDD systems, is integrated into the design. All voltage controlled oscillators (VCOs) and loop filter components are integrated.

The core of the AD9363 can be powered directly from a 1.3 V regulator. The IC is controlled via a standard 4-wire serial port and four real-time I/O control pins. Comprehensive power-down modes are included to minimize power consumption during normal use. The AD9363 is packaged in a 10 mm × 10 mm, 144-ball chip scale package ball grid array (CSP_BGA).

Rev. D

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REVISION HISTORY

11/2016—Revision D: Initial Version

SPECIFICATIONS

Electrical characteristics at VDD_GPO = 3.3 V, VDD_INTERFACE = 1.8 V, and all other VDDx pins (VDDA1P3_TX_LO, VDDA1P3_TX_VCO_LDO, VDDA1P3_RX_LO, VDDA1P3_RX_VCO_LDO, VDDA1P3_RX_RF, VDDA1P3_RX_TX, VDDA1P3_TX_LO_BUFFER, VDDA1P3_TX_SYNTH, VDDA1P3_RX_SYNTH, VDDD1P3_DIG, and VDDA1P3_BB) = 1.3 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVERS, GENERAL						
Center Frequency		325		3800	MHz	
Rx Bandwidth				20	MHz	
Gain						
Minimum			0		dB	
Maximum			74.5		dB	At 800 MHz
			73.0		dB	At 2300 MHz (RX1A_x, RX2A_x)
			72.0		dB	At 2300 MHz (RX1B_x, RX1C_x, RX2B_x, RX2C_x)
Gain Step			1		dB	
Received Signal Strength Indicator	RSSI					
Range			100		dB	
Accuracy			±2		dB	
RECEIVERS, 800 MHz						
Noise Figure	NF		2.5		dB	Maximum Rx gain
Third-Order Input Intermodulation Intercept Point	IIP3		−18		dBm	Maximum Rx gain
Second-Order Input Intermodulation Intercept Point	IIP2		40		dBm	Maximum Rx gain
Local Oscillator (LO) Leakage			−122		dBm	At Rx front-end input
Quadrature						
Gain Error			0.2		%	
Phase Error			0.2		Degrees	
Modulation Accuracy (EVM)			−34		dB	19.2 MHz reference clock
Input Return Loss	S11		−10		dB	
RX1x_x to RX2x_x Isolation						
RX1A_x to RX2A_x, RX1C_x to RX2C_x			70		dB	
RX1B_x to RX2B_x			55		dB	
RX2_x to RX1_x Isolation						
RX2A_x to RX1A_x, RX2C_x to RX1C_x			70		dB	
RX2B_x to RX1B_x			55		dB	
RECEIVERS, 2.4 GHz						
Noise Figure	NF		3		dB	Maximum Rx gain
Third-Order Input Intermodulation Intercept Point	IIP3		−14		dBm	Maximum Rx gain
Second-Order Input Intermodulation Intercept Point	IIP2		45		dBm	Maximum Rx gain
Local Oscillator (LO) Leakage			−110		dBm	At Rx front-end input
Quadrature						
Gain Error			0.2		%	
Phase Error			0.2		Degrees	
Modulation Accuracy (EVM)			−34		dB	40 MHz reference clock
Input Return Loss	S11		−10		dB	
RX1x_x to RX2x_x Isolation						
RX1A_x to RX2A_x, RX1C_x to RX2C_x			65		dB	
RX1B_x to RX2B_x			50		dB	

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RX2x_x to RX1x_x Isolation						
RX2A_x to RX1A_x, RX2C_x to RX1C_x			65		dB	
RX2B_x to RX1B_x			50		dB	
RECEIVERS, 3.5 GHz						
Noise Figure	NF		3.3		dB	Maximum Rx gain
Third-Order Input Intermodulation Intercept Point	IIP3		−15		dBm	Maximum Rx gain
Second-Order Input Intermodulation Intercept Point	IIP2		44		dBm	Maximum Rx gain
Local Oscillator (LO) Leakage			−100		dBm	At Rx front-end input
Quadrature						
Gain Error			0.2		%	
Phase Error			0.2		Degrees	
Modulation Accuracy (EVM)			−34		dB	40 MHz reference clock
Input Return Loss	S11		−10		dB	
RX1x_x to RX2x_x Isolation						
RX1A_x to RX2A_x, RX1C_x to RX2C_x			60		dB	
RX1B_x to RX2B_x			48		dB	
RX2x_x to RX1x_x Isolation						
RX2A_x to RX1A_x, RX2C_x to RX1C_x			60		dB	
RX2B_x to RX1B_x			48		dB	
TRANSMITTERS, GENERAL						
Center Frequency		325		3800	MHz	
Tx Bandwidth				20	MHz	
Power Control Range			90		dB	
Power Control Resolution			0.25		dB	
TRANSMITTERS, 800 MHz						
Output Return Loss	S22		−10		dB	
Maximum Output Power			8		dBm	1 MHz tone into 50 Ω load
Modulation Accuracy (EVM)			−34		dB	19.2 MHz reference clock
Third-Order Output Intermodulation Intercept Point	OIP3		23		dBm	
Carrier Leakage			−50		dBc	0 dB attenuation
			−32		dBc	40 dB attenuation
Noise Floor			−157		dBm/Hz	90 MHz offset
Isolation						
TX1x_x to TX2x_x			50		dB	
TX2x_x to TX1x_x			50		dB	
TRANSMITTERS, 2.4 GHz						
Output Return Loss	S22		−10		dB	
Maximum Output Power			7.5		dBm	1 MHz tone into 50 Ω load
Modulation Accuracy (EVM)			−34		dB	40 MHz reference clock
Third-Order Output Intermodulation Intercept Point	OIP3		19		dBm	
Carrier Leakage			−50		dBc	0 dB attenuation
			−32		dBc	40 dB attenuation
Noise Floor			−156		dBm/Hz	90 MHz offset
Isolation						
TX1x_x to TX2x_x			50		dB	
TX2x_x to TX1x_x			50		dB	
TRANSMITTERS, 3.5 GHz						
Output Return Loss	S22		−10		dB	
Maximum Output Power			7.0		dBm	1 MHz tone into 50 Ω load
Modulation Accuracy (EVM)			−34		dB	40 MHz reference clock

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Third-Order Output Intermodulation Intercept Point	OIP3		18		dBm	
Carrier Leakage			−50		dBc	0 dB attenuation
			−31		dBc	40 dB attenuation
Noise Floor			−154		dBm/Hz	90 MHz offset
Isolation						
TX1 to TX2			50		dB	
TX2 to TX1			50		dB	

[1] When referencing a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

Table 2.

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TX MONITOR INPUTS (TX_MON1, TX_MON2)						
Maximum Input Level			4		dBm	
Dynamic Range			66		dB	
Accuracy			1		dB	
LO SYNTHESIZER						
LO Frequency Step			2.4		Hz	2.4 GHz, 40 MHz reference clock
Integrated Phase Noise			0.3		°rms	100 Hz to 100 MHz
REFERENCE CLOCK (REF_CLK)						REF_CLK is the input to the XTALN pin
Input Frequency Range		10		80	MHz	External oscillator
Input Signal Level			1.3		V p-p	AC-coupled external oscillator
AUXILIARY ADC						
Resolution			12		Bits	
Input Voltage						
Minimum			0.05		V	
Maximum			VDDA1P3_BB − 0.05		V	
AUXILIARY DAC						
Resolution			10		Bits	
Output Voltage						
Minimum			0.5		V	
Maximum			VDD_GPO − 0.3		V	
Output Current			10		mA	
DIGITAL SPECIFICATIONS (CMOS)						
Logic Inputs						
Input Voltage High		VDD_INTERFACE × 0.8		VDD_INTERFACE	V	
Input Voltage Low		0		VDD_INTERFACE × 0.2	V	
Input Current High		−10		+10	μA	
Input Current Low		−10		+10	μA	
Logic Outputs						
Output Voltage High		VDD_INTERFACE × 0.8		VDD_INTERFACE	V	
Output Voltage Low		0		VDD_INTERFACE × 0.2	V	
DIGITAL SPECIFICATIONS (LVDS)						
Logic Inputs						
Input Voltage Range		825		1575	mV	Each differential input in the pair
Input Differential Voltage Threshold		−100		+100	mV	

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Receiver Differential Input Impedance			100		Ω	
Logic Outputs						
Output Voltage High				1375	mV	
Output Voltage Low		1025			mV	
Output Differential Voltage		150			mV	Programmable in 75 mV steps
Output Offset Voltage			1200		mV	
GENERAL-PURPOSE OUTPUTS						
Output Voltage High		VDD_GPO × 0.8		VDD_GPO	V	
Output Voltage Low		0		VDD_GPO × 0.2	V	
Output Current			10		mA	
SPI TIMING						VDD_INTERFACE = 1.8 V
SPI_CLK						
Period	t_{CP}	20			ns	
Pulse Width	t_{MP}	9			ns	
SPI_EN Setup to First SPI_CLK Rising Edge	t_{SC}	1			ns	
Last SPI_CLK Falling Edge to SPI_ENB Hold	t_{HC}	0			ns	
SPI_DI						
Data Input Setup to SPI_CLK	t_S	2			ns	
Data Input Hold to SPI_CLK	t_H	1			ns	
SPI_CLK Rising Edge to Output Data Delay						
4-Wire Mode	t_{CO}	3		8	ns	
3-Wire Mode	t_{CO}	3		8	ns	
Bus Turnaround Time, Read (Master)	t_{HZM}	t_H		$t_{CO\ (MAX)}$	ns	After baseband processors (BBP) drives the last address bit
Bus Turnaround Time, Read (Slave)	t_{HZS}	0		$t_{CO\ (MAX)}$	ns	After AD9363 drives the last data bit
DIGITAL DATA TIMING (CMOS), VDD_INTERFACE = 1.8 V						
DATA_CLK_x Clock Period	t_{CP}	16.276			ns	61.44 MHz
DATA_CLK_x and FB_CLK_x Pulse Width	t_{MP}	45% of t_{CP}		55% of t_{CP}	ns	
Tx Data						TX_FRAME_x, P0_Dx, and P1_Dx
Setup to FB_CLK_x	t_{STX}	1			ns	
Hold to FB_CLK_x	t_{HTX}	0			ns	
DATA_CLK_x to Data Bus Output Delay	t_{DDRX}	0		1.5	ns	
DATA_CLK_x to RX_FRAME_x Delay	t_{DDDV}	0		1.0	ns	
Pulse Width						
ENABLE	t_{ENPW}	t_{CP}			ns	
TXNRX	$t_{TXNRXPW}$	t_{CP}			ns	FDD independent enable state machine (ENSM) mode
TXNRX Setup to ENABLE	$t_{TXNRXSU}$	0			ns	TDD ENSM mode
Bus Turnaround Time						TDD mode
Before Rx	t_{RPRE}	2 × t_{CP}			ns	
After Rx	t_{RPST}	2 × t_{CP}			ns	
Capacitive Load			3		pF	
Capacitive Input			3		pF	

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL DATA TIMING (CMOS), VDD_INTERFACE = 2.5 V						
DATA_CLK_x Clock Period	t_{CP}	16.276			ns	61.44 MHz
DATA_CLK_x and FB_CLK_x Pulse Width	t_{MP}	45% of t_{CP}		55% of t_{CP}	ns	
Tx Data						TX_FRAME_x, P0_Dx, and P1_Dx
Setup to FB_CLK_x	t_{STX}	1			ns	
Hold to FB_CLK_x	t_{HTX}	0			ns	
DATA_CLK_x to Data Bus Output Delay	t_{DDRX}	0.25		1.25	ns	
DATA_CLK_x to RX_FRAME_x Delay	t_{DDDV}	0.25		1.25	ns	
Pulse Width						
ENABLE	t_{ENPW}	t_{CP}			ns	
TXNRX	$t_{TXNRXPW}$	t_{CP}			ns	FDD independent ENSM mode
TXNRX Setup to ENABLE	$t_{TXNRXSU}$	0			ns	TDD ENSM mode
Bus Turnaround Time						TDD mode
Before Rx	t_{RPRE}	$2 \times t_{CP}$			ns	
After Rx	t_{RPST}	$2 \times t_{CP}$			ns	
Capacitive Load			3		pF	
Capacitive Input			3		pF	
DIGITAL DATA TIMING (LVDS)						
DATA_CLK_x Clock Period	t_{CP}	4.069			ns	245.76 MHz
DATA_CLK_x and FB_CLK_x Pulse Width	t_{MP}	45% of t_{CP}		55% of t_{CP}	ns	
Tx Data						TX_FRAME_x and TX_Dx
Setup to FB_CLK_x	t_{STX}	1			ns	
Hold to FB_CLK_x	t_{HTX}	0			ns	
DATA_CLK_x to Data Bus Output Delay	t_{DDRX}	0		1.5	ns	
DATA_CLK_x to RX_FRAME_x Delay	t_{DDDV}	0		1.0	ns	
Pulse Width						
ENABLE	t_{ENPW}	t_{CP}			ns	
TXNRX	$t_{TXNRXPW}$	t_{CP}			ns	FDD independent ENSM mode
TXNRX Setup to ENABLE	$t_{TXNRXSU}$	0			ns	TDD ENSM mode
Bus Turnaround Time						
Before Rx	t_{RPRE}	$2 \times t_{CP}$			ns	
After Rx	t_{RPST}	$2 \times t_{CP}$			ns	
Capacitive Load			3		pF	
Capacitive Input			3		pF	
SUPPLY CHARACTERISTICS						
1.3 V Main Supply		1.267	1.3	1.33	V	
VDD_INTERFACE Supply						
CMOS		1.2		2.5	V	
LVDS		1.8		2.5	V	
VDD_GPO Supply		1.3	3.3	3.465	V	When unused, must be set to 1.3 V
Current Consumption						
VDDx, Sleep Mode			180		µA	Sum of all input currents
VDD_GPO			50		µA	No load

[1] When referencing a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

CURRENT CONSUMPTION—VDD_INTERFACE

Table 3. VDD_INTERFACE = 1.2 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SLEEP MODE		45		μA	Power applied, device disabled
ONE Rx CHANNEL, ONE Tx CHANNEL, DOUBLE DATA RATE (DDR)					
LTE10					
Single Port		2.9		mA	30.72 MHz data clock, CMOS
Dual Port		2.7		mA	15.36 MHz data clock, CMOS
LTE20					
Dual Port		5.2		mA	30.72 MHz data clock, CMOS
TWO Rx CHANNELS, TWO Tx CHANNELS, DDR					
LTE3					
Dual Port		1.3		mA	7.68 MHz data clock, CMOS
LTE10					
Single Port		4.6		mA	61.44 MHz data clock, CMOS
Dual Port		5.0		mA	30.72 MHz data clock, CMOS
LTE20					
Dual Port		8.2		mA	61.44 MHz data clock, CMOS
GSM					
Dual Port		0.2		mA	1.08 MHz data clock, CMOS
WiMAX 8.75 MHz					
Dual Port		3.3		mA	20 MHz data clock, CMOS
WiMAX 10 MHz					
Single Port					
TDD Rx		0.5		mA	22.4 MHz data clock, CMOS
TDD Tx		3.6		mA	22.4 MHz data clock, CMOS
FDD		3.8		mA	44.8 MHz data clock, CMOS
WiMAX 20 MHz					
Dual Port					
FDD		6.7		mA	44.8 MHz data clock, CMOS

Table 4. VDD_INTERFACE = 1.8 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SLEEP MODE		84		µA	Power applied, device disabled
ONE Rx CHANNEL, ONE Tx CHANNEL, DDR					
LTE10					
Single Port		4.5		mA	30.72 MHz data clock, CMOS
Dual Port		4.1		mA	15.36 MHz data clock, CMOS
LTE20					
Dual Port		8.0		mA	30.72 MHz data clock, CMOS
TWO Rx CHANNELS, TWO Tx CHANNELS, DDR					
LTE3					
Dual Port		2.0		mA	7.68 MHz data clock, CMOS
LTE10					
Single Port		8.0		mA	61.44 MHz data clock, CMOS
Dual Port		7.5		mA	30.72 MHz data clock, CMOS
LTE20					
Dual Port		14.0		mA	61.44 MHz data clock, CMOS
GSM					
Dual Port		0.3		mA	1.08 MHz data clock, CMOS
WiMAX 8.75 MHz					
Dual Port		5.0		mA	20 MHz data clock, CMOS
WiMAX 10 MHz					
Single Port					
TDD Rx		0.7		mA	22.4 MHz data clock, CMOS
TDD Tx		5.6		mA	22.4 MHz data clock, CMOS
FDD		6.0		mA	44.8 MHz data clock, CMOS
WiMAX 20 MHz					
Dual Port					
FDD		10.7		mA	44.8 MHz data clock, CMOS

Table 5. VDD_INTERFACE = 2.5 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SLEEP MODE		150		µA	Power applied, device disabled
ONE Rx CHANNEL, ONE Tx CHANNEL, DDR					
LTE10					
Single Port		6.5		mA	30.72 MHz data clock, CMOS
Dual Port		6.0		mA	15.36 MHz data clock, CMOS
LTE20					
Dual Port		11.5		mA	30.72 MHz data clock, CMOS
TWO Rx CHANNELS, TWO Tx CHANNELS, DDR					
LTE3					
Dual Port		3.0		mA	7.68 MHz data clock, CMOS
LTE10					
Single Port		11.5		mA	61.44 MHz data clock, CMOS
Dual Port		10.0		mA	30.72 MHz data clock, CMOS
LTE20					
Dual Port		20.0		mA	61.44 MHz data clock, CMOS
GSM					
Dual Port		0.5		mA	1.08 MHz data clock, CMOS
WiMAX 8.75 MHz					
Dual Port		7.3		mA	20 MHz data clock, CMOS
WiMAX 10 MHz					
Single Port					
TDD Rx		1.3		mA	22.4 MHz data clock, CMOS
TDD Tx		8.0		mA	22.4 MHz data clock, CMOS
FDD		8.7		mA	44.8 MHz data clock, CMOS
WiMAX 20 MHz					
Dual Port					
FDD		15.3		mA	44.8 MHz data clock, CMOS

CURRENT CONSUMPTION—VDDx (COMBINATION OF ALL 1.3 V SUPPLIES)

Table 6. TDD Mode, 800 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ONE Rx CHANNEL					Continuous Rx
5 MHz BW		180		mA	
10 MHz BW		210		mA	
20 MHz BW		260		mA	
TWO Rx CHANNELS					Continuous Rx
5 MHz BW		265		mA	
10 MHz BW		315		mA	
20 MHz BW		405		mA	
ONE Tx CHANNEL					Continuous Tx
5 MHz BW					
7 dBm		340		mA	
−27 dBm		190		mA	
10 MHz BW					
7 dBm		360		mA	
−27 dBm		220		mA	
20 MHz BW					
7 dBm		400		mA	
−27 dBm		250		mA	
TWO Tx CHANNELS					Continuous Tx
5 MHz BW					
7 dBm		550		mA	
−27 dBm		260		mA	
10 MHz BW					
7 dBm		600		mA	
−27 dBm		310		mA	
20 MHz BW					
7 dBm		660		mA	
−27 dBm		370		mA	

Table 7. TDD Mode, 2.4 GHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ONE Rx CHANNEL					Continuous Rx
5 MHz BW		175		mA	
10 MHz BW		200		mA	
20 MHz BW		240		mA	
TWO Rx CHANNELS					Continuous Rx
5 MHz BW		260		mA	
10 MHz BW		305		mA	
20 MHz BW		390		mA	
ONE Tx CHANNEL					Continuous Tx
5 MHz BW					
7 dBm		350		mA	
−27 dBm		160		mA	
10 MHz BW					
7 dBm		380		mA	
−27 dBm		220		mA	
20 MHz BW					
7 dBm		410		mA	
−27 dBm		260		mA	
TWO Tx CHANNELS					Continuous Tx
5 MHz BW					
7 dBm		580		mA	
−27 dBm		280		mA	
10 MHz BW					
7 dBm		635		mA	
−27 dBm		330		mA	
20 MHz BW					
7 dBm		690		mA	
−27 dBm		390		mA	

Table 8. FDD Mode, 800 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ONE Rx CHANNEL, ONE Tx CHANNEL					Continuous Rx and Tx
5 MHz BW					
7 dBm		490		mA	
−27 dBm		345		mA	
10 MHz BW					
7 dBm		540		mA	
−27 dBm		395		mA	
20 MHz BW					
7 dBm		615		mA	
−27 dBm		470		mA	
TWO Rx CHANNELS, ONE Tx CHANNEL					Continuous Rx and Tx
5 MHz BW					
7 dBm		555		mA	
−27 dBm		410		mA	
10 MHz BW					
7 dBm		625		mA	
−27 dBm		480		mA	
20 MHz BW					
7 dBm		740		mA	
−27 dBm		600		mA	
ONE Rx CHANNEL, TWO Tx CHANNELS					Continuous Rx and Tx
5 MHz BW					
7 dBm		685		mA	
−27 dBm		395		mA	
10 MHz BW					
7 dBm		755		mA	
−27 dBm		465		mA	
20 MHz BW					
7 dBm		850		mA	
−27 dBm		570		mA	
TWO Rx CHANNELS, TWO Tx CHANNELS					
5 MHz BW					
7 dBm		790		mA	
−27 dBm		495		mA	
10 MHz BW					
7 dBm		885		mA	
−27 dBm		590		mA	
20 MHz BW					
7 dBm		1020		mA	
−27 dBm		730		mA	

Table 9. FDD Mode, 2.4 GHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ONE Rx CHANNEL, ONE Tx CHANNEL					Continuous Rx and Tx
5 MHz BW					
7 dBm		500		mA	
−27 dBm		350		mA	
10 MHz BW					
7 dBm		540		mA	
−27 dBm		390		mA	
20 MHz BW					
7 dBm		620		mA	
−27 dBm		475		mA	
TWO Rx CHANNELS, ONE Tx CHANNEL					Continuous Rx and Tx
5 MHz BW					
7 dBm		590		mA	
−27 dBm		435		mA	
10 MHz BW					
7 dBm		660		mA	
−27 dBm		510		mA	
20 MHz BW					
7 dBm		770		mA	
−27 dBm		620		mA	
ONE Rx CHANNEL, TWO Tx CHANNELS					Continuous Rx and Tx
5 MHz BW					
7 dBm		730		mA	
−27 dBm		425		mA	
10 MHz BW					
7 dBm		800		mA	
−27 dBm		500		mA	
20 MHz BW					
7 dBm		900		mA	
−27 dBm		600		mA	
TWO Rx CHANNELS, TWO Tx CHANNELS					Continuous Rx and Tx
5 MHz BW					
7 dBm		820		mA	
−27 dBm		515		mA	
10 MHz BW					
7 dBm		900		mA	
−27 dBm		595		mA	
20 MHz BW					
7 dBm		1050		mA	
−27 dBm		740		mA	

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
VDDx to VSSx	−0.3 V to +1.4 V
VDD_INTERFACE to VSSx	−0.3 V to +3.0 V
VDD_GPO to VSSx	−0.3 V to +3.9 V
Logic Inputs and Outputs to VSSx	−0.3 V to VDD_INTERFACE + 0.3 V
Input Current to Any Pin Except Supplies	±10 mA
RF Inputs (Peak Power)	2.5 dBm
Tx Monitor Input Power (Peak Power)	9 dBm
Package Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Maximum Junction Temperature (T_{JMAX})	110°C
Temperature Range	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
Reflow	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

REFLOW PROFILE

The AD9363 reflow profile is in accordance with the JEDEC JESD20 criteria for Pb-free devices. The maximum reflow temperature is 260°C.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment.

Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

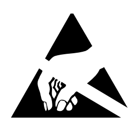
θ_{JC} is the junction to case thermal resistance.

Table 11. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[2]	θ_{JC}[3]	Unit
BC-144-7[1]	0	32.3	9.6	°C/W
	1.0	29.6	N/A[4]	°C/W
	2.5	27.8	N/A[4]	°C/W

[1] Per JEDEC JESD51-7, plus JEDEC JESD51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD-883, Method 1012.1.
[4] N/A means not applicable.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	RX2A_N	RX2A_P	DNC	VSSA	TX_MON2	VSSA	TX2A_N	TX2A_P	TX2B_N	TX2B_P	VDDA1P1_ TX_VCO	VSSA
B	VSSA	VSSA	AUXDAC1	GPO_3	GPO_2	GPO_1	GPO_0	VDD_GPO	VDDA1P3_ TX_LO	VDDA1P3_ TX_VCO_ LDO	TX_VCO_ LDO_OUT	VSSA
C	RX2C_P	VSSA	AUXDAC2	TEST/ ENABLE	CTRL_IN0	CTRL_IN1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
D	RX2C_N	VDDA1P3_ RX_RF	VDDA1P3_ RX_TX	CTRL_OUT0	CTRL_IN3	CTRL_IN2	P0_D9/ TX_D4_P	P0_D7/ TX_D3_P	P0_D5/ TX_D2_P	P0_D3/ TX_D1_P	P0_D1/ TX_D0_P	VSSD
E	RX2B_P	VDDA1P3_ RX_LO	VDDA1P3_ TX_LO_ BUFFER	CTRL_OUT1	CTRL_OUT2	CTRL_OUT3	P0_D11/ TX_D5_P	P0_D8/ TX_D4_N	P0_D6/ TX_D3_N	P0_D4/ TX_D2_N	P0_D2/ TX_D1_N	P0_D0/ TX_D0_N
F	RX2B_N	VDDA1P3_ RX_VCO_ LDO	VSSA	CTRL_OUT6	CTRL_OUT5	CTRL_OUT4	VSSD	P0_D10/ TX_D5_N	VSSD	FB_CLK_P	VSSD	VDDD1P3_ DIG
G	VSSA	RX_VCO_ LDO_OUT	VDDA1P1_ RX_VCO	CTRL_OUT7	EN_AGC	ENABLE	RX_ FRAME_N	RX_ FRAME_P	TX_ FRAME_P	FB_CLK_N	DATA_ CLK_P	VSSD
H	RX1B_P	VSSA	VSSA	TXNRX	VSSA	VSSA	VSSD	P1_D11/ RX_D5_P	TX_ FRAME_N	VSSD	DATA_ CLK_N	VDD_ INTERFACE
J	RX1B_N	VSSA	VDDA1P3_ RX_SYNTH	SPI_DI	SPI_CLK	CLK_OUT	P1_D10/ RX_D5_N	P1_D9/ RX_D4_P	P1_D7/ RX_D3_P	P1_D5/ RX_D2_P	P1_D3/ RX_D1_P	P1_D1/ RX_D0_P
K	RX1C_P	VSSA	VDDA1P3_ TX_SYNTH	VDDA1P3_ BB	RESET	SPI_EN	P1_D8/ RX_D4_N	P1_D6/ RX_D3_N	P1_D4/ RX_D2_N	P1_D2/ RX_D1_N	P1_D0/ RX_D0_N	VSSD
L	RX1C_N	VSSA	VSSA	RBIAS	AUXADC	SPI_DO	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
M	RX1A_P	RX1A_N	DNC	VSSA	TX_MON1	VSSA	TX1A_P	TX1A_N	TX1B_P	TX1B_N	DNC	XTALN

ANALOG I/O
DIGITAL I/O
DO NOT CONNECT
DC POWER
GROUND

10558-002

Figure 2. Pin Configuration, Top View

Table 12. Pin Function Descriptions

Pin No.	Type[1]	Mnemonic	Description
A1, A2	I	RX2A_N, RX2A_P	Receive Channel 2 Differential A Inputs. Alternatively, each pin can be used as a single-ended input. Unused pins must be tied to ground.
A3, M3, M11	NC	DNC	Do Not Connect. Do not connect to these pins.
A4, A6, A12, B1, B2, B12, C2, C7 to C12, F3, G1, H2, H3, H5, H6, J2, K2, L2, L3, L7 to L12, M4, M6	GND	VSSA	Analog Ground. Tie these pins directly to the VSSD digital ground on the PCB (one ground plane).
A5	I	TX_MON2	Transmit Channel 2 Power Monitor Input. If this pin is unused, tie it to ground.
A7, A8	O	TX2A_N, TX2A_P	Transmit Channel 2 Differential A Outputs. Unused pins must be tied to 1.3 V.
A9, A10	O	TX2B_N, TX2B_P	Transmit Channel 2 Differential B Outputs. Unused pins must be tied to 1.3 V.
A11	P	VDDA1P1_TX_VCO	Transmit VCO Supply Input. Connect to B11.
B3	O	AUXDAC1	Auxiliary DAC 1 Output. If using the auxiliary DAC, connect a 0.1 μF capacitor from this pin to ground.
B4 to B7	O	GPO_3 to GPO_0	3.3 V Capable General-Purpose Outputs.
B8	I	VDD_GPO	2.5 V to 3.3 V Supply for the AUXDAC and General-Purpose Output Pins. If the VDD_GPO supply is not used, this supply must be set to 1.3 V.
B9	I	VDDA1P3_TX_LO	Transmit Local Oscillator (LO) 1.3 V Supply Input.
B10	I	VDDA1P3_TX_VCO_LDO	Transmit VCO LDO 1.3 V Supply Input. Connect to B9.
B11	O	TX_VCO_LDO_OUT	Transmit VCO LDO Output. Connect to A11 and to a 1 μF bypass capacitor in series with a 1 Ω resistor to ground.
C1, D1	I	RX2C_P, RX2C_N	Receive Channel 2 Differential C Inputs. Alternatively, use each pin as a single-ended input. Unused pins must be tied to ground.
C3	O	AUXDAC2	Auxiliary DAC 2 Output. If using the auxiliary DAC, connect a 0.1 μF capacitor from this pin to ground.
C4	I	TEST/ENABLE	Test Input. Ground this pin for normal operation.
C5, C6, D5, D6	I	CTRL_IN0 to CTRL_IN3	Control Inputs. Use these pins for manual Rx gain and Tx attenuation control.

Pin No.	Type[1]	Mnemonic	Description
D2	I	VDDA1P3_RX_RF	Receiver 1.3 V Supply Input. Connect to D3.
D3	I	VDDA1P3_RX_TX	Receiver and Transmitter 1.3 V Supply Input.
D4, E4 to E6, F4 to F6, G4	O	CTRL_OUT0, CTRL_OUT1 to CTRL_OUT3, CTRL_OUT6 to CTRL_OUT4, CTRL_OUT7	Control Outputs. These pins are multipurpose outputs that have programmable functionality.
D7	I/O	P0_D9/TX_D4_P	Digital Data Port 0, Data Bit 9/Transmit Differential Input Bus, Data Bit 4. This is a dual function pin. As P0_D9, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D4_P, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
D8	I/O	P0_D7/TX_D3_P	Digital Data Port 0, Data Bit 7/Transmit Differential Input Bus, Data Bit 3. This is a dual function pin. As P0_D7, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D3_P, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
D9	I/O	P0_D5/TX_D2_P	Digital Data Port 0, Data Bit 5/Transmit Differential Input Bus, Data Bit 2. This is a dual function pin. As P0_D5, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D2_P, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
D10	I/O	P0_D3/TX_D1_P	Digital Data Port 0, Data Bit 3/Transmit Differential Input Bus, Data Bit 1. This is a dual function pin. As P0_D3, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D1_P, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
D11	I/O	P0_D1/TX_D0_P	Digital Data Port 0, Data Bit 1/Transmit Differential Input Bus, Data Bit 0. This is a dual function pin. As P0_D1, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D0_P, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
D12, F7, F9, F11, G12, H7, H10, K12	GND	VSSD	Digital Ground. Tie these pins directly to the VSSA analog ground on the PCB (one ground plane).
E1, F1	I	RX2B_P, RX2B_N	Receive Channel 2 Differential B Inputs. Alternatively, each pin can be used as a single-ended input. Unused pins must be tied to ground.
E2	I	VDDA1P3_RX_LO	Receive LO 1.3 V Supply Input.
E3	I	VDDA1P3_TX_LO_BUFFER	Transmitter LO Buffer 1.3 V Supply Input.
E7	I/O	P0_D11/TX_D5_P	Digital Data Port 0, Data Bit 11/Transmit Differential Input Bus, Data Bit 5. This is a dual function pin. As P0_D11, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D5_P, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
E8	I/O	P0_D8/TX_D4_N	Digital Data Port 0, Data Bit 8/Transmit Differential Input Bus, Data Bit 4. This is a dual function pin. As P0_D8, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D4_N, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
E9	I/O	P0_D6/TX_D3_N	Digital Data Port 0, Data Bit 6/Transmit Differential Input Bus, Data Bit 3. This is a dual function pin. As P0_D6, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D3_N, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
E10	I/O	P0_D4/TX_D2_N	Digital Data Port 0, Data Bit 4/Transmit Differential Input Bus, Data Bit 2. This is a dual function pin. As P0_D4, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D2_N, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
E11	I/O	P0_D2/TX_D1_N	Digital Data Port 0, Data Bit 2/Transmit Differential Input Bus, Data Bit 1. This is a dual function pin. As P0_D2, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D1_N, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
E12	I/O	P0_D0/TX_D0_N	Digital Data Port 0, Data Bit 0/Transmit Differential Input Bus, Data Bit 0. This is a dual function pin. As P0_D0, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D0_N, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
F2	I	VDDA1P3_RX_VCO_LDO	Receive VCO LDO 1.3 V Supply Input. Connect to E2.

Pin No.	Type[1]	Mnemonic	Description
F8	I/O	P0_D10/TX_D5_N	Digital Data Port 0, Data Bit 10/Transmit Differential Input Bus, Data Bit 5. This is a dual function pin. As P0_D10, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, as TX_D5_N, it functions as part of the LVDS 6-bit Tx differential input bus with internal LVDS termination.
F10, G10	I	FB_CLK_P, FB_CLK_N	Feedback Clock Inputs. These pins receive the FB_CLK signal that clocks in Tx data. In CMOS mode, use FB_CLK_P as the input and tie FB_CLK_N to ground.
F12	I	VDDD1P3_DIG	1.3 V Digital Supply Input.
G2	O	RX_VCO_LDO_OUT	Receive VCO LDO Output. Connect to G3 and to a 1 μF bypass capacitor in series with a 1 Ω resistor to ground.
G3	I	VDDA1P1_RX_VCO	Receive VCO Supply Input. Connect to G2.
G5	I	EN_AGC	Manual Control Input for Automatic Gain Control (AGC).
G6	I	ENABLE	Control Input. This pin moves the device through various operational states.
G7, G8	O	RX_FRAME_N, RX_FRAME_P	Receive Digital Data Framing Outputs. These pins transmit the RX_FRAME signal that indicates whether the Rx output data is valid. In CMOS mode, use RX_FRAME_P as the output and leave RX_FRAME_N unconnected.
G9, H9	I	TX_FRAME_P, TX_FRAME_N	Transmit Digital Data Framing Inputs. These pins receive the TX_FRAME signal that indicates when Tx data is valid. In CMOS mode, use TX_FRAME_P as the input and tie TX_FRAME_N to ground.
G11, H11	O	DATA_CLK_P, DATA_CLK_N	Receive Data Clock Outputs. These pins transmit the DATA_CLK signal that the BBP uses to clock the Rx data. In CMOS mode, use DATA_CLK_P as the output and leave DATA_CLK_N unconnected.
H1, J1	I	RX1B_P, RX1B_N	Receive Channel 1 Differential B Inputs. Alternatively, use each pin as a single-ended input. Unused pins must be tied to ground.
H4	I	TXNRX	Enable State Machine Control Signal. This pin controls the data port bus direction. A logic low selects the Rx direction; a logic high selects the Tx direction.
H8	I/O	P1_D11/RX_D5_P	Digital Data Port P1, Data Bit 11/Receive Differential Output Bus, Data Bit 5. This is a dual function pin. As P1_D11, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D5_P, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
H12	I	VDD_INTERFACE	1.2 V to 2.5 V Supply for Digital I/O Pins (1.8 V to 2.5 V in LVDS Mode).
J3	I	VDDA1P3_RX_SYNTH	Receiver Synthesizer 1.3 V Supply Input.
J4	I	SPI_DI	SPI Serial Data Input.
J5	I	SPI_CLK	SPI Clock Input.
J6	O	CLK_OUT	Output Clock. This pin can be configured to output either a buffered version of the external input clock (the digital controlled crystal oscillator (DCXO)) or a divided-down version of the internal ADC sample clock (ADC_CLK).
J7	I/O	P1_D10/RX_D5_N	Digital Data Port 1, Data Bit 10/Receive Differential Output Bus, Data Bit 5. This is a dual function pin. As P1_D10, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D5_N, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
J8	I/O	P1_D9/RX_D4_P	Digital Data Port 1, Data Bit 9/Receive Differential Output Bus, Data Bit 4. This is a dual function pin. As P1_D9, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D4_P, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
J9	I/O	P1_D7/RX_D3_P	Digital Data Port 1, Data Bit 7/Receive Differential Output Bus, Data Bit 3. This is a dual function pin. As P1_D7, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D3_P, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
J10	I/O	P1_D5/RX_D2_P	Digital Data Port 1, Data Bit 5/Receive Differential Output Bus, Data Bit 2. This is a dual function pin. As P1_D5, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D2_P, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
J11	I/O	P1_D3/RX_D1_P	Digital Data Port 1, Data Bit 3/Receive Differential Output Bus, Data Bit 1. This is a dual function pin. As P1_D3, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D1_P, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.

Pin No.	Type[1]	Mnemonic	Description
J12	I/O	P1_D1/RX_D0_P	Digital Data Port 1, Data Bit 1/Receive Differential Output Bus, Data Bit 0. This is a dual function pin. As P1_D1, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D0_P, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
K1, L1	I	RX1C_P, RX1C_N	Receive Channel 1 Differential C Inputs. Alternatively, use each pin as a single-ended input. Tie unused pins to ground.
K3	I	VDDA1P3_TX_SYNTH	Transmitter Synthesizer 1.3 V Supply Input. Connect this pin to a 1.3 V regulator through a separate trace to a common supply point.
K4	I	VDDA1P3_BB	Baseband 1.3 V Supply Input. Connect this pin to a 1.3 V regulator through a separate trace to a common supply point.
K5	I	$\overline{\text{RESET}}$	Asynchronous Reset Input. A logic low resets the device.
K6	I	$\overline{\text{SPI\_EN}}$	SPI Enable. Set this pin to logic low to enable the SPI bus.
K7	I/O	P1_D8/RX_D4_N	Digital Data Port 1, Data Bit 8/Receive Differential Output Bus, Data Bit 4. This is a dual function pin. As P1_D8, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D4_N, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
K8	I/O	P1_D6/RX_D3_N	Digital Data Port 1, Data Bit 6/Receive Differential Output Bus, Data Bit 3. This is a dual function pin. As P1_D6, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D3_N, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
K9	I/O	P1_D4/RX_D2_N	Digital Data Port 1, Data Bit 4/Receive Differential Output Bus, Data Bit 2. This is a dual function pin. As P1_D4, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D2_N, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
K10	I/O	P1_D2/RX_D1_N	Digital Data Port 1, Data Bit 2/Receive Differential Output Bus, Data Bit 1. This is a dual function pin. As P1_D2, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D1_N, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
K11	I/O	P1_D0/RX_D0_N	Digital Data Port 1, Data Bit 0/Receive Differential Output Bus, Data Bit 0. This is a dual function pin. As P1_D0, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, as RX_D0_N, it functions as part of the LVDS 6-bit Rx differential output bus with internal LVDS termination.
L4	I	RBIAS	Bias Input Reference. Connect this pin through a 14.3 kΩ (1% tolerance) resistor to ground.
L5	I	AUXADC	Auxiliary ADC Input. If this pin is unused, tie it to ground.
L6	O	SPI_DO	SPI Serial Data Output in 4-Wire Mode, High-Z in 3-Wire Mode.
M1, M2	I	RX1A_P, RX1A_N	Receive Channel 1 Differential A Inputs. Alternatively, use each pin as a single-ended input. Tie unused pins to ground.
M5	I	TX_MON1	Transmit Channel 1 Power Monitor Input. If this pin is unused, tie it to ground.
M7, M8	O	TX1A_P, TX1A_N	Transmit Channel 1 Differential A Outputs. Tie unused pins to 1.3 V.
M9, M10	O	TX1B_P, TX1B_N	Transmit Channel 1 Differential B Outputs. Tie unused pins to 1.3 V.
M12	I	XTALN	Reference Frequency Connection. Connect the external clock source to XTALN.

[1] I is input, NC is not connected, GND is ground, O is output, P is power, and I/O is input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

ATTEN is the attenuation setting. f_{LO_RX} and f_{LO_TX} are the receive and transmit local oscillator frequencies, respectively.

800 MHZ FREQUENCY BAND

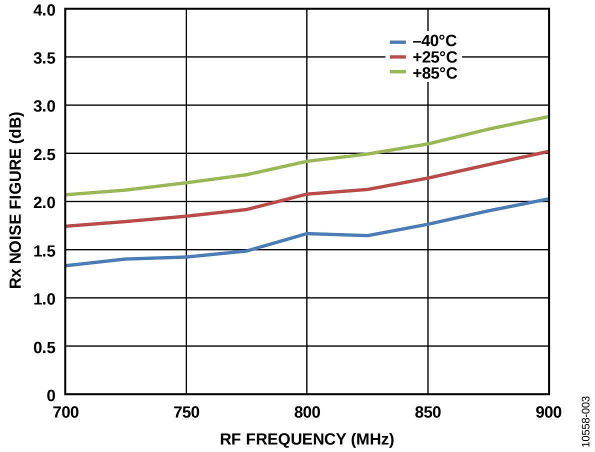


Figure 3. Rx Noise Figure vs. RF Frequency

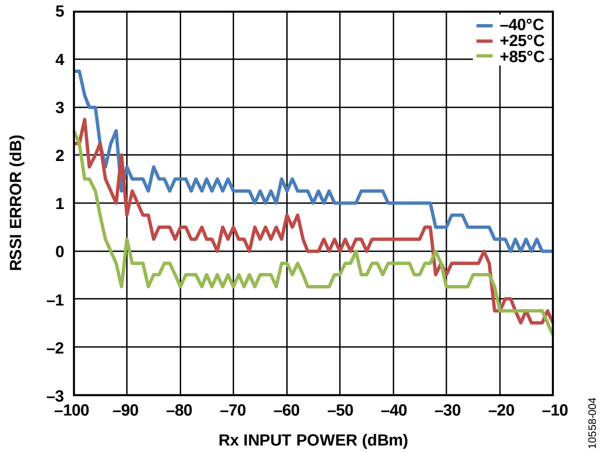


Figure 4. RSSI Error vs. Rx Input Power, LTE 10 MHz Modulation (Referenced to −50 dBm Input Power at 800 MHz)

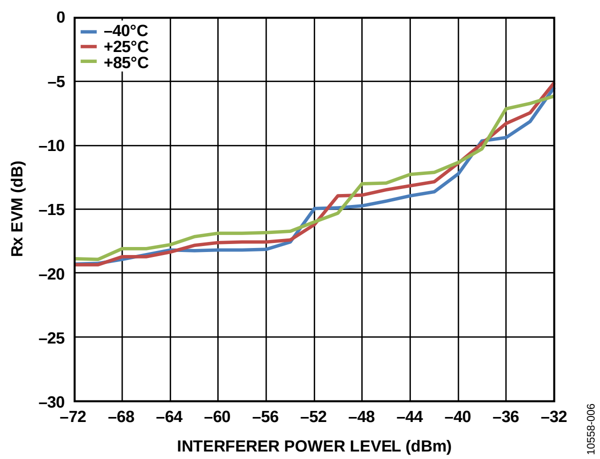


Figure 5. Rx EVM vs. Interferer Power Level, LTE 10 MHz Signal of Interest with P_{IN} = −82 dBm, 5 MHz Orthogonal Frequency Division Multiplexing (OFDM) Blocker at 7.5 MHz Offset

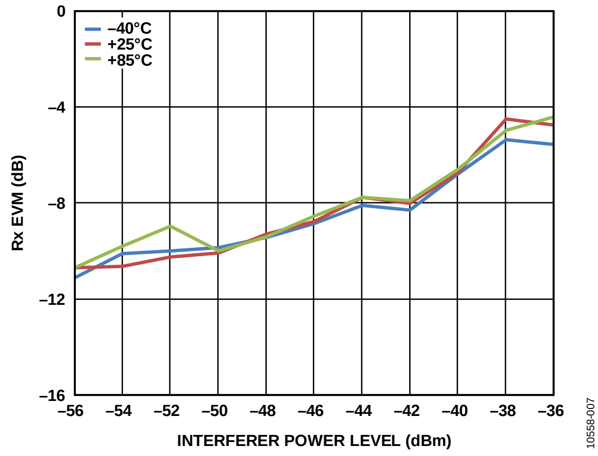


Figure 6. Rx EVM vs. Interferer Power Level, LTE 10 MHz Signal of Interest with P_{IN} = −90 dBm, 5 MHz OFDM Blocker at 17.5 MHz Offset

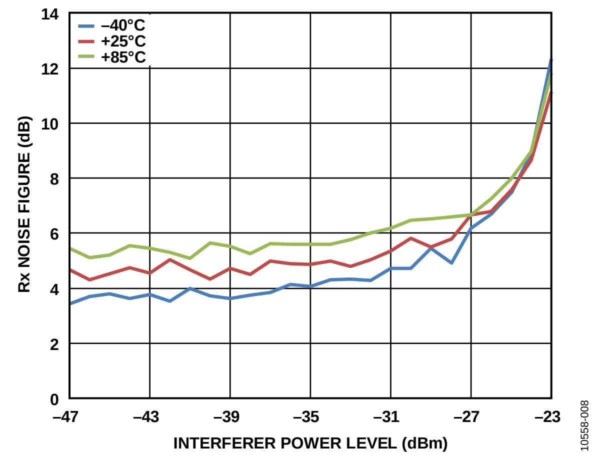


Figure 7. Rx Noise Figure vs. Interferer Power Level, Enhanced Data Rates for GSM Evolution (EDGE) Signal of Interest with P_{IN} = −90 dBm, Continuous Wave (CW) Blocker at 3 MHz Offset, Gain Index = 64

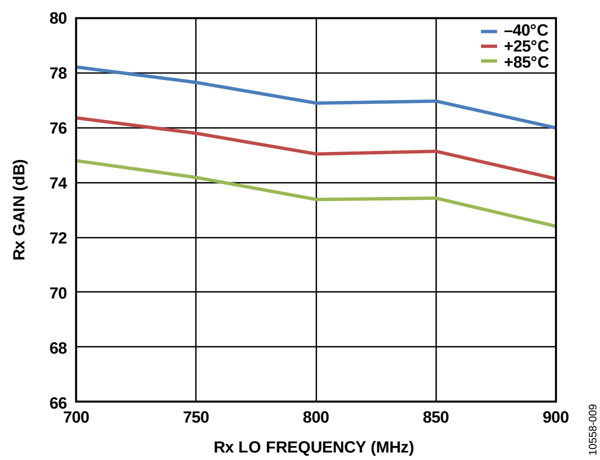


Figure 8. Rx Gain vs. Rx LO Frequency, Gain Index = 76 (Maximum Setting)

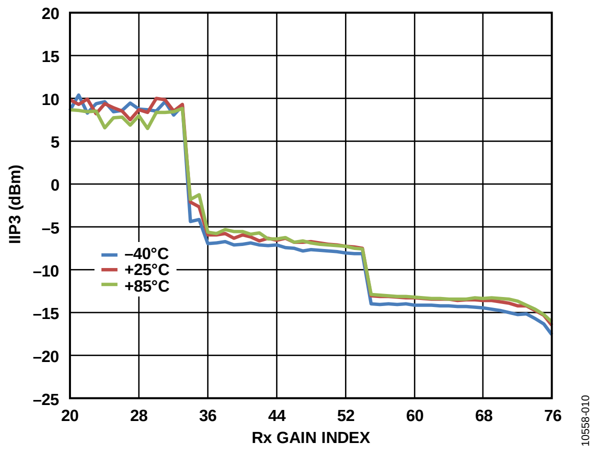


Figure 9. Third-Order Input Intercept Point (IIP3) vs. Rx Gain Index, f1 = 1.45 MHz, f2 = 2.89 MHz, GSM Mode

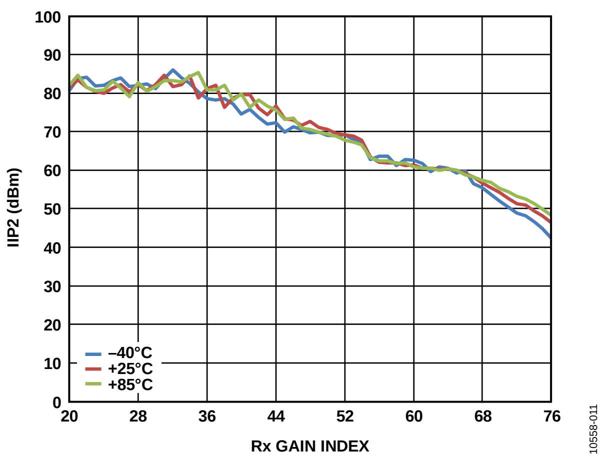


Figure 10. Second-Order Input Intercept Point (IIP2) vs. Rx Gain Index, f1 = 2.00 MHz, f2 = 2.01 MHz, GSM Mode

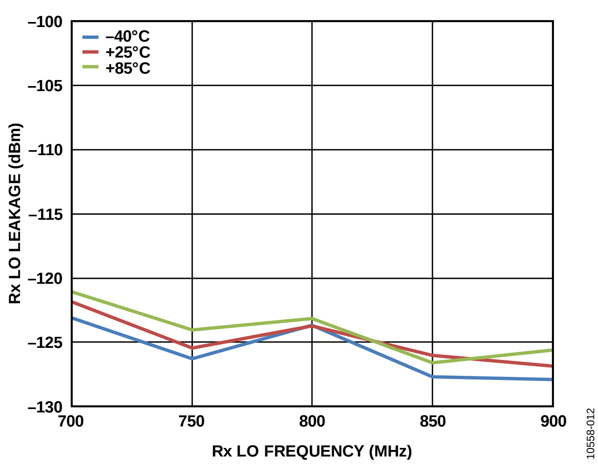


Figure 11. Rx LO Leakage vs. Rx LO Frequency

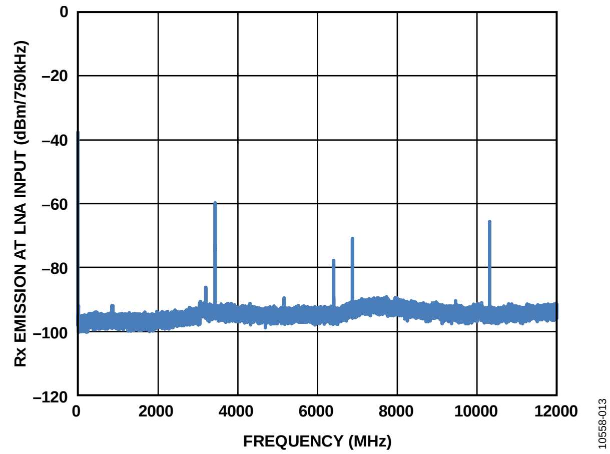


Figure 12. Rx Emission at LNA Input vs. Frequency, DC to 12 GHz, f_{LO_RX} = 800 MHz, LTE 10 MHz, f_{LO_TX} = 860 MHz

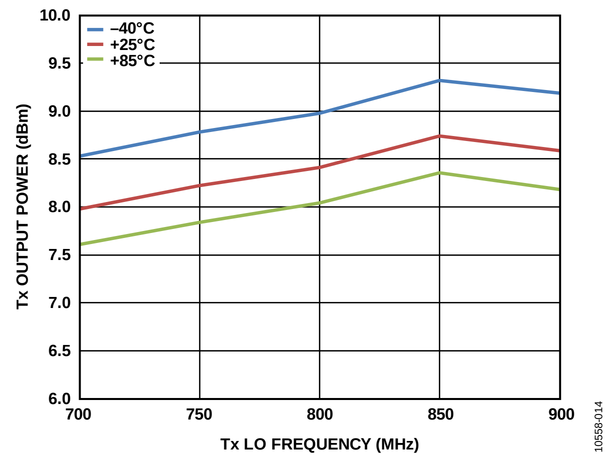


Figure 13. Tx Output Power vs. Tx LO Frequency, Attenuation Setting = 0 dB, Single-Tone Output

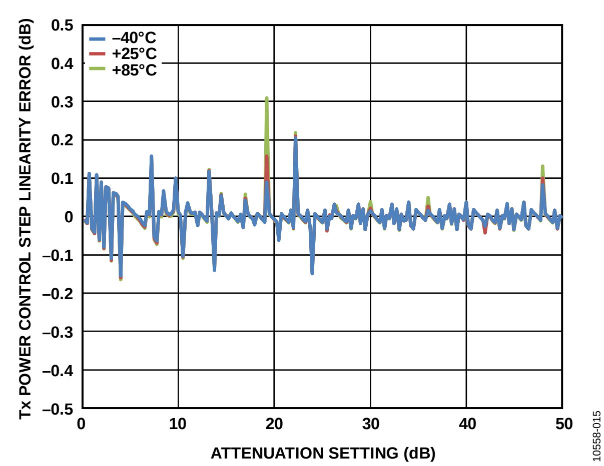


Figure 14. Tx Power Control Step Linearity Error vs. Attenuation Setting

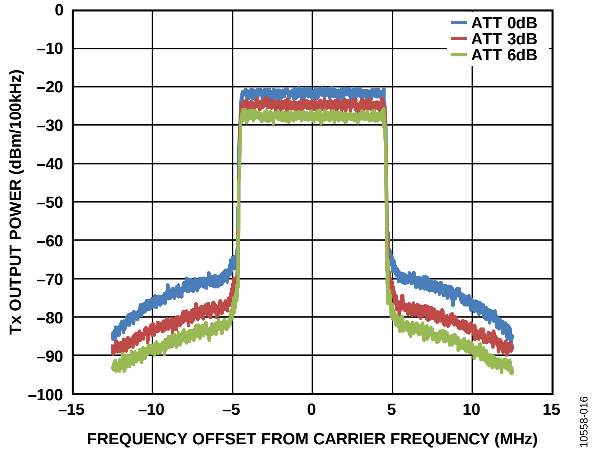


Figure 15. Tx Output Power vs. Frequency Offset from Carrier Frequency, f_{LO_TX} = 800 MHz, LTE 10 MHz Downlink (Digital Attenuation Variations Shown)

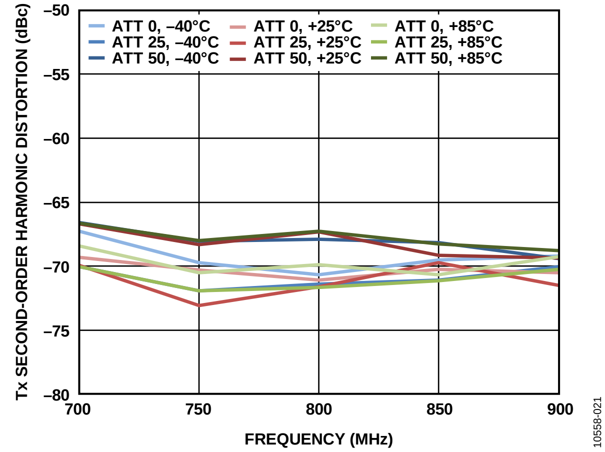


Figure 18. Tx Second-Order Harmonic Distortion (HD2) vs. Frequency

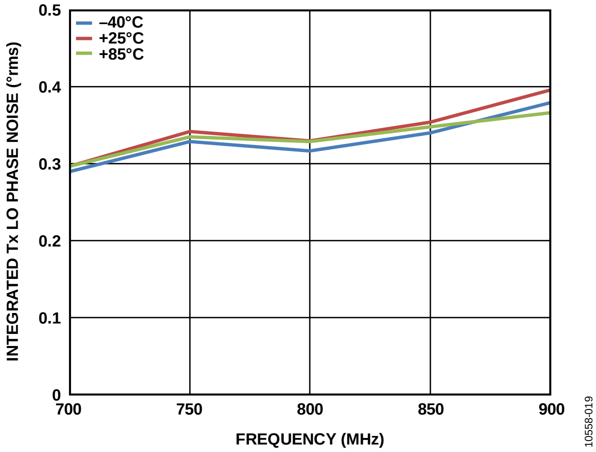


Figure 16. Integrated Tx LO Phase Noise vs. Frequency, 19.2 MHz REF_CLK

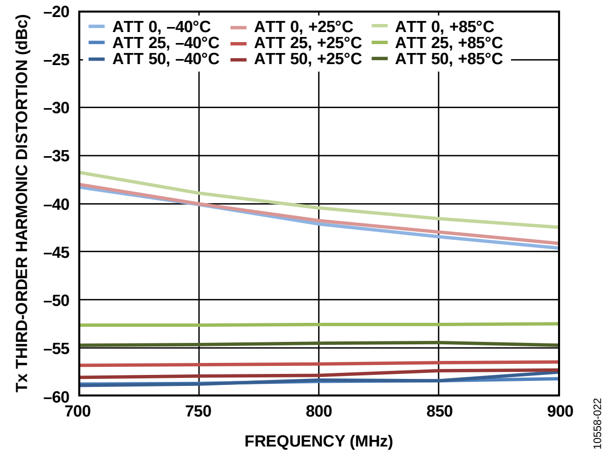


Figure 19. Tx Third-Order Harmonic Distortion (HD3) vs. Frequency

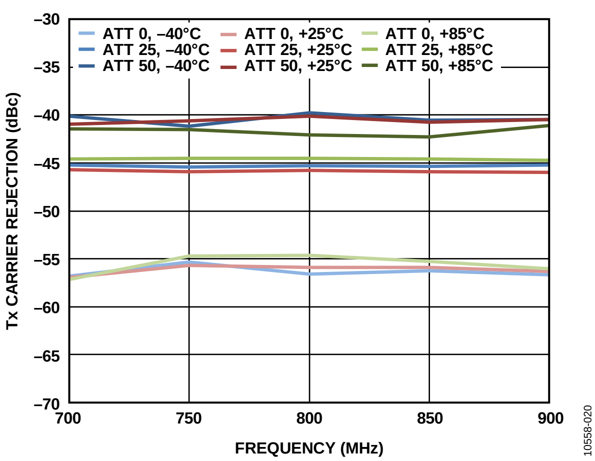


Figure 17. Tx Carrier Rejection vs. Frequency

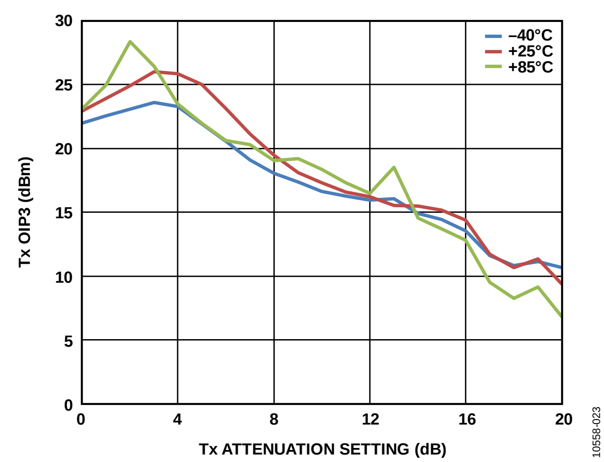


Figure 20. Tx Third-Order Output Intercept Point (OIP3) vs. Tx Attenuation Setting

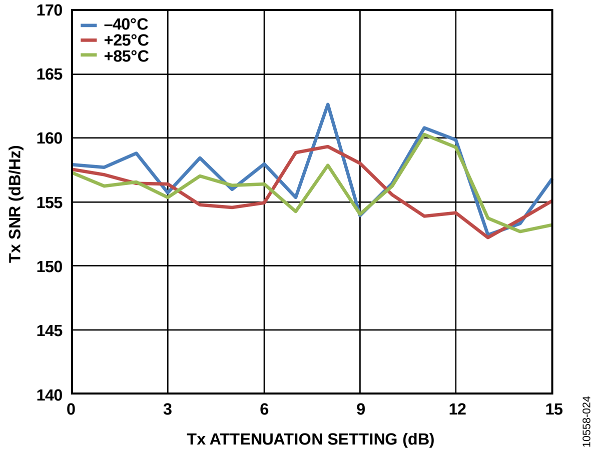


Figure 21. Tx Signal-to-Noise Ratio (SNR) vs. Tx Attenuation Setting, LTE 10 MHz Signal of Interest with Noise Measured at 90 MHz Offset

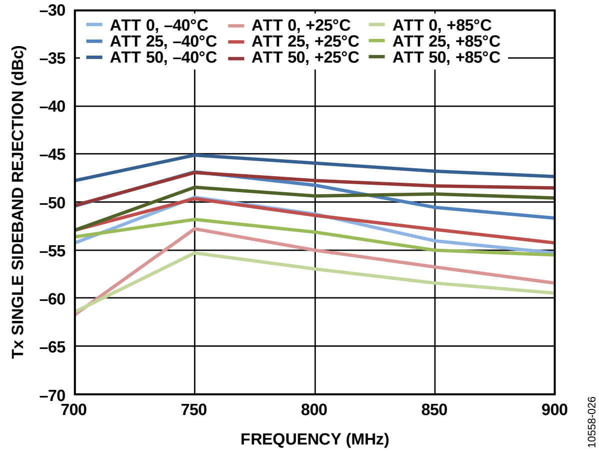


Figure 22. Tx Single Sideband Rejection vs. Frequency, 1.5375 MHz Offset

2.4 GHZ FREQUENCY BAND

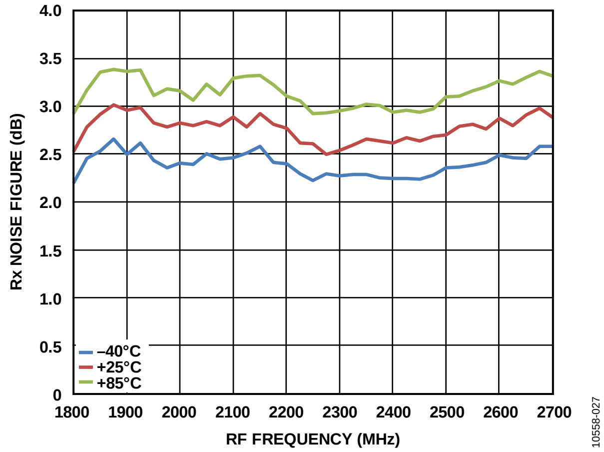


Figure 23. Rx Noise Figure vs. RF Frequency

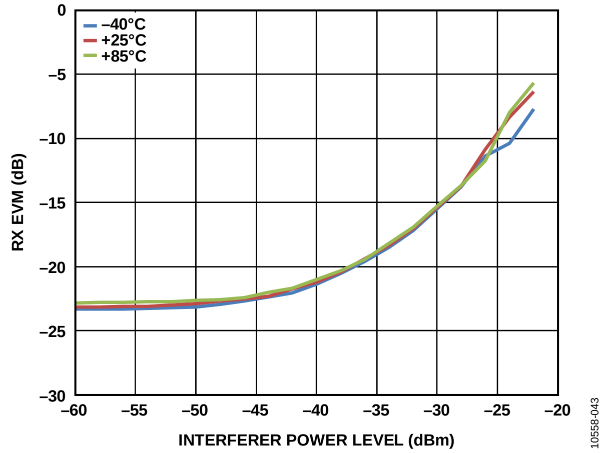


Figure 26. Rx EVM vs. Interferer Power Level, LTE 20 MHz Signal of Interest with P_{IN} = −75 dBm, LTE 20 MHz Blocker at 40 MHz Offset

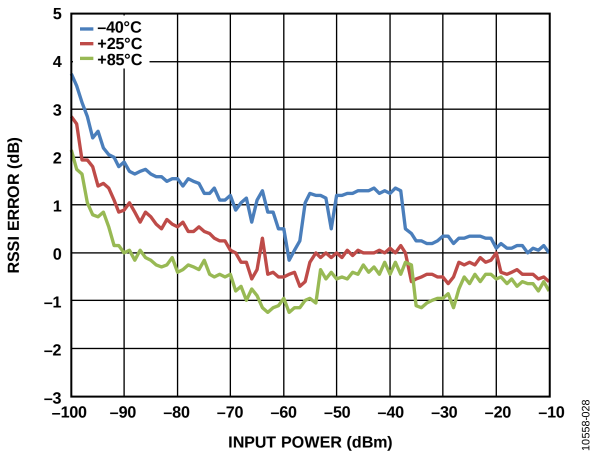


Figure 24. RSSI Error vs. Input Power (Referenced to −50 dBm Input Power at 2.4 GHz)

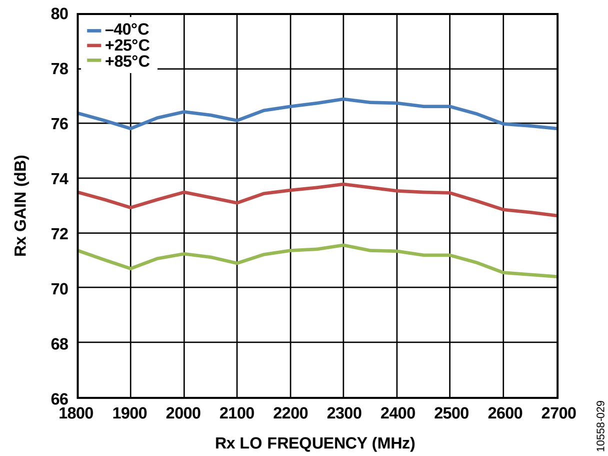


Figure 27. Rx Gain vs. Rx LO Frequency, Gain Index = 76 (Maximum Setting)

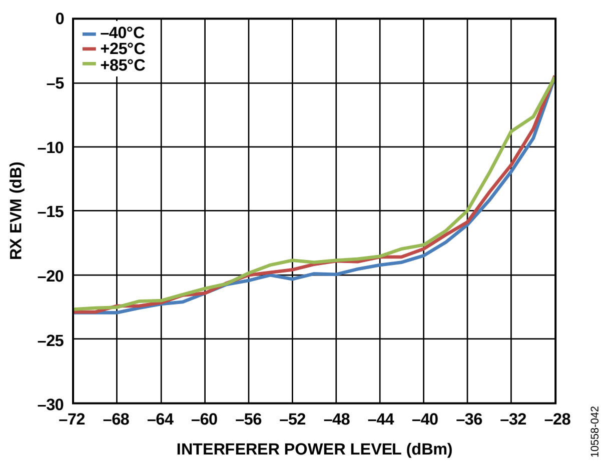


Figure 25. Rx EVM vs. Interferer Power Level, LTE 20 MHz Signal of Interest with P_{IN} = −75 dBm, LTE 20 MHz Blocker at 20 MHz Offset

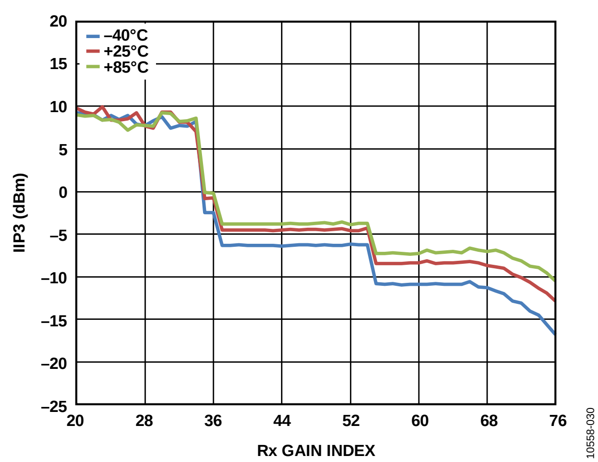


Figure 28. Third-Order Input Intercept Point (IIP3) vs. Rx Gain Index, f1 = 30 MHz, f2 = 61 MHz

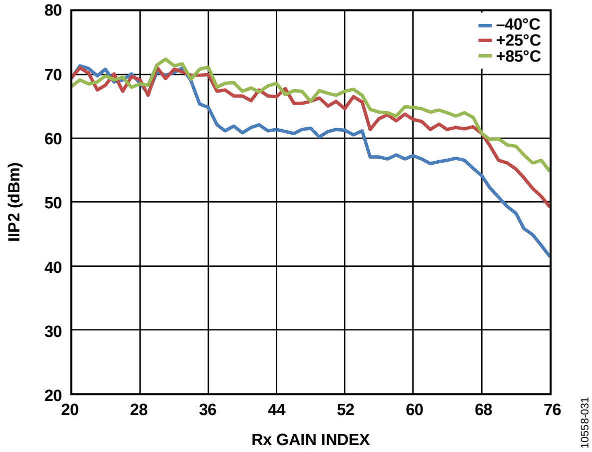


Figure 29. Second-Order Input Intercept Point (IIP2) vs. Rx Gain Index, f1 = 60 MHz, f2 = 61 MHz

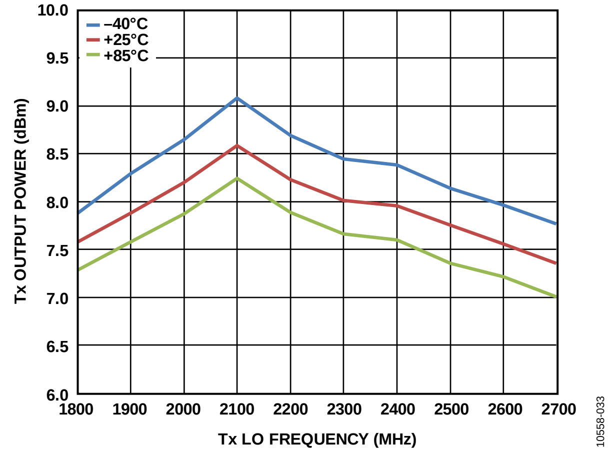


Figure 32. Tx Output Power vs. Tx LO Frequency, Attenuation Setting = 0 dB, Single-Tone Output

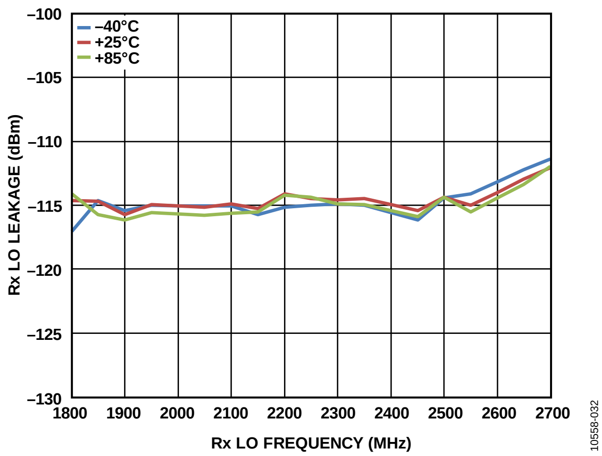


Figure 30. Rx Local Oscillator (LO) Leakage vs. Rx LO Frequency

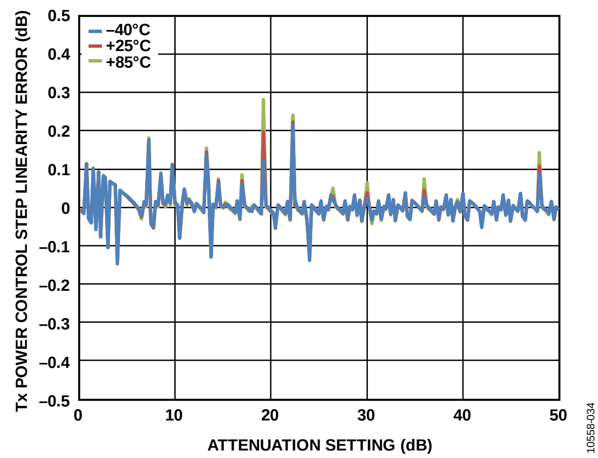


Figure 33. Tx Power Control Step Linearity Error vs. Attenuation Setting

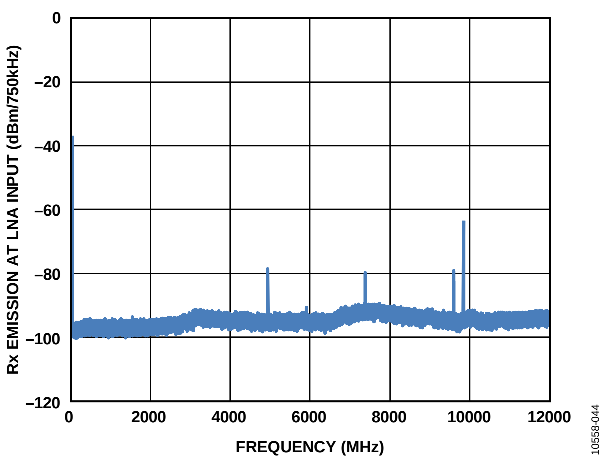


Figure 31. Rx Emission at LNA Input vs. Frequency, DC to 12 GHz, f_{LO_RX} = 2.4 GHz, LTE 20 MHz, f_{LO_TX} = 2.46 GHz

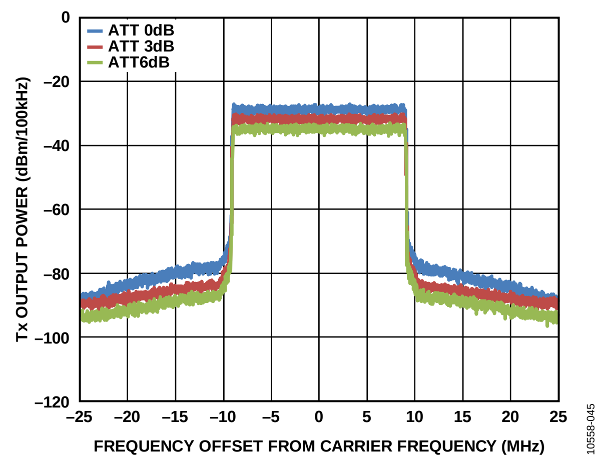


Figure 34. Tx Output Power vs. Frequency Offset from Carrier Frequency, f_{LO_TX} = 2.3 GHz, LTE 20 MHz Downlink (Digital Attenuation Variations Shown)

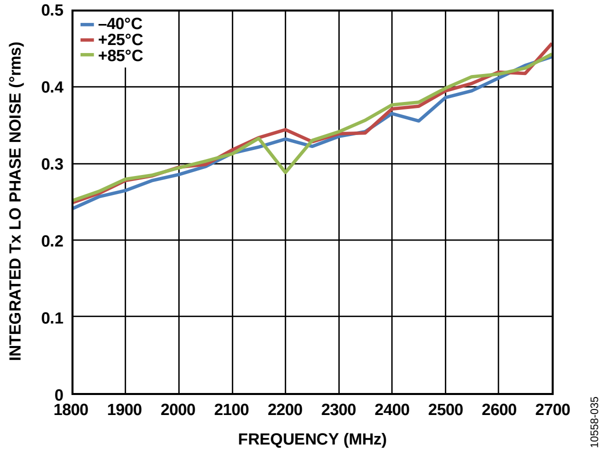


Figure 35. Integrated Tx LO Phase Noise vs. Frequency, 40 MHz REF_CLK

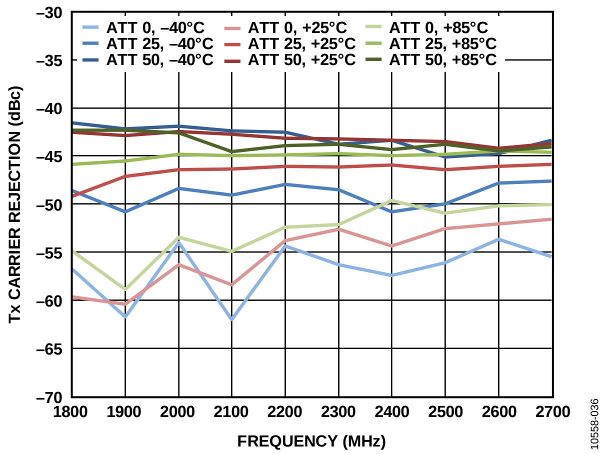


Figure 36. Tx Carrier Rejection vs. Frequency

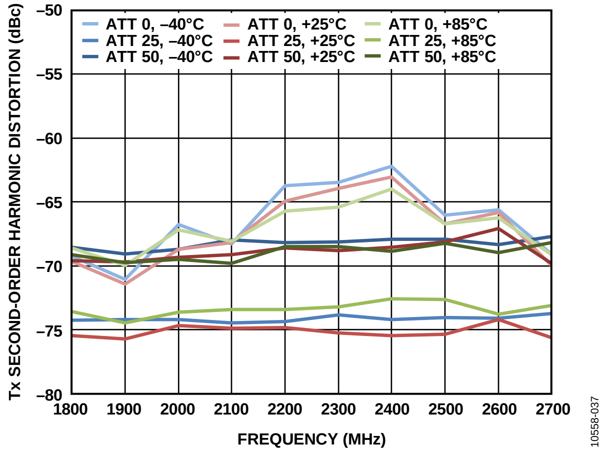


Figure 37. Tx Second-Order Harmonic Distortion (HD2) vs. Frequency

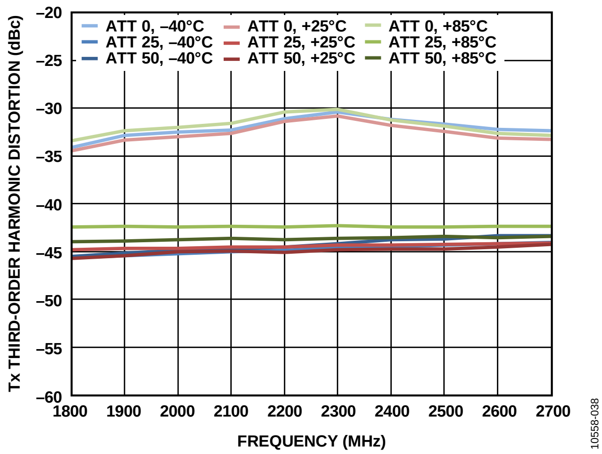


Figure 38. Tx Third-Order Harmonic Distortion (HD3) vs. Frequency

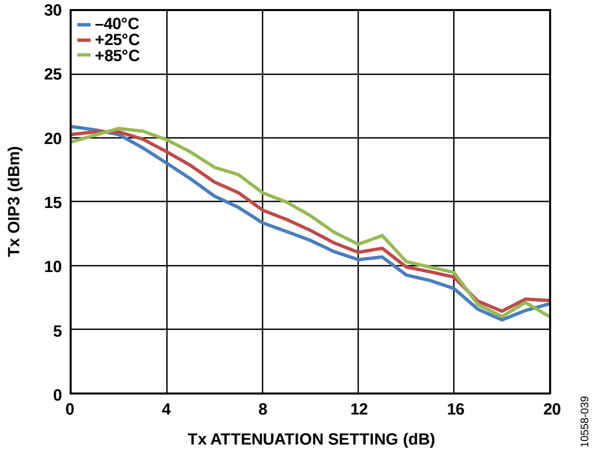


Figure 39. Tx Third-Order Output Intercept Point (OIP3) vs. Tx Attenuation Setting

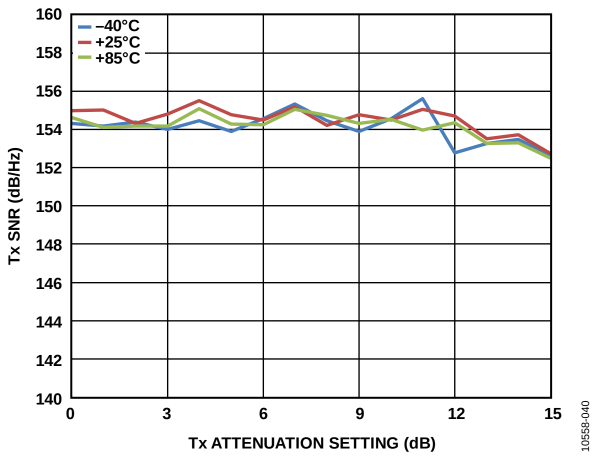


Figure 40. Tx Signal-to-Noise Ratio (SNR) vs. Tx Attenuation Setting, LTE 20 MHz Signal of Interest with Noise Measured at 90 MHz Offset

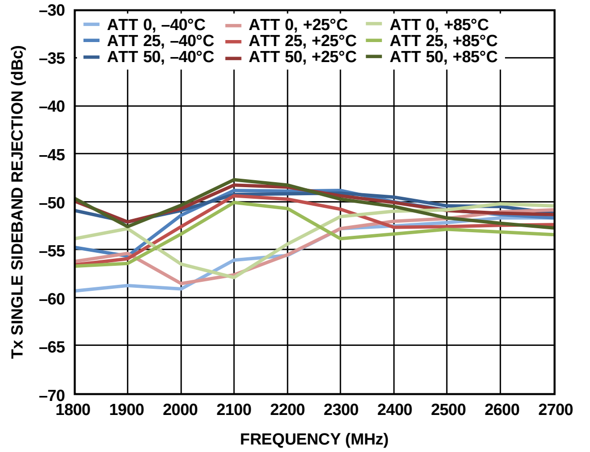


Figure 41. Tx Single Sideband Rejection vs. Frequency, 3.075 MHz Offset

THEORY OF OPERATION

GENERAL

The AD9363 is a highly integrated radio frequency (RF) transceiver capable of being configured for a wide range of applications. The device integrates all RF, mixed-signal, and digital blocks necessary to provide all transceiver functions in a single device. Programmability allows this broadband transceiver to be adapted for use with multiple communication standards, including FDD and TDD systems. This programmability also allows the device to interface to various BBPs using a single 12-bit parallel data port, dual 12-bit parallel data ports, or a 12-bit low voltage differential signaling (LVDS) interface.

The AD9363 also provides self calibration and AGC systems to maintain a high performance level under varying temperatures and input signal conditions. In addition, the device includes several test modes that allow system designers to insert test tones and create internal loopback modes to debug their designs during prototyping and optimize their radio configuration for a specific application.

RECEIVER

The receiver section contains all blocks necessary to receive RF signals and convert them to digital data that is usable by a BBP. Two independently controlled channels can receive signals from different sources, allowing the device to be used in multiple input, multiple output (MIMO) systems while sharing a common frequency synthesizer.

Each channel has three inputs that can be multiplexed to the signal chain, making the AD9363 suitable for use in diversity systems with multiple antenna inputs. The receiver is a direct conversion system that contains a low noise amplifier (LNA) followed by matched in-phase (I) and quadrature (Q) amplifiers, mixers, and band shaping filters that downconvert received signals to baseband for digitization. External LNAs can also be interfaced to the device, allowing designers the flexibility to customize the receiver front end for their specific application.

Gain control is achieved by following a preprogrammed gain index map that distributes gain among the blocks for optimal performance at each level. This gain control can be achieved by enabling the internal AGC in either fast or slow mode or by using manual gain control, allowing the BBP to make the gain adjustments as needed. Additionally, each channel contains independent RSSI measurement capability, dc offset tracking, and all circuitry necessary for self calibration.

The receivers include 12-bit, sigma-delta (Σ-Δ) ADCs and adjustable sample rates that produce data streams from the received signals. The digitized signals can be conditioned further by a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sample rate of each digital filter block can also be adjusted by changing the decimation factors to produce the desired output data rate.

TRANSMITTER

The transmitter section consists of two identical and independently controlled channels that provide all digital processing, mixed-signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data received from the BBP passes through a fully programmable 128-tap FIR filter with interpolation options. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each 12-bit DAC has an adjustable sampling rate. Both the I and Q channels are fed to the RF block for upconversion.

After being converted to baseband analog signals, the I and Q signals are filtered to remove sampling artifacts and provide band shaping, and then they are passed to the upconversion mixers. At this point, the I and Q signals are recombined and modulated on the carrier frequency for transmission to the output stage. The output stage provides attenuation control that provides a range of output levels while keeping the output impedance at 50 Ω. A wide range of attenuation adjustment with fine granularity is included to help designers optimize SNR.

Self calibration circuitry is included in the transmit channel to provide internal adjustment capability. The transmitter also provides a Tx monitor block that receives the transmitter output and routes it back through an unused receiver channel to the BBP for signal monitoring. The Tx monitor blocks are available only in TDD mode operation while the receiver is idle.

CLOCK INPUT OPTIONS

The AD9363 uses a reference clock provided by an external oscillator or clock distribution device (such as the AD9548) connected to the XTALN pin. The frequency of this reference clock can vary from 10 MHz to 80 MHz. This reference clock supplies the synthesizer blocks that generate all data clocks, sample clocks, and local oscillators inside the device.

SYNTHESIZERS

RF PLLs

The AD9363 contains two identical synthesizers to generate the required LO signals for the RF signal paths—one for the receiver and one for the transmitter. PLL synthesizers are fractional N designs that incorporate completely integrated VCOs and loop filters. In TDD mode, the synthesizers turn on and off as appropriate for the Rx and Tx frames. In FDD mode, the Tx PLL and the Rx PLL can be activated at the same time. These PLLs require no external components.

BB PLL

The AD9363 also contains a baseband PLL (BB PLL) synthesizer that generates all baseband related clock signals. These signals include the ADC and DAC sampling clocks, the DATA_CLK signal (see the Digital Data Interface section), and all data framing signals. The BB PLL is programmed from 700 MHz to 1400 MHz based on the data rate and sample rate requirements of the system.

DIGITAL DATA INTERFACE

The AD9363 data interface uses parallel data ports (P0 and P1) to transfer data between the device and the BBP. The data ports can be configured in either single-ended CMOS format or differential LVDS format. Both formats can be configured in multiple arrangements to match system requirements for data ordering and data port connections. These arrangements include single port data bus, dual port data bus, single data rate, double data rate, and various combinations of data ordering to transmit data from different channels across the bus at appropriate times.

Bus transfers are controlled using simple hardware handshake signaling. The two ports can be operated in either bidirectional (TDD) mode or in full duplex (FDD) mode, where half the bits are used for transmitting data and half are used for receiving data. The interface can also be configured to use only one of the data ports for applications that do not require high data rates and require fewer interface pins.

DATA_CLK Signal

The AD9363 outputs the DATA_CLK signal that the BBP uses to sample receiver data. The signal is synchronized with the receiver data such that data transitions occur out of phase with DATA_CLK. The DATA_CLK can be set to a rate that provides single data rate (SDR) timing, where data is sampled on each rising clock edge, or it can be set to provide double data rate (DDR) timing, where data is captured on both rising and falling clock edges. SDR or DDR timing applies to operation using either a single port or both ports.

FB_CLK Signal

For transmit data, the interface uses the FB_CLK signal as the timing reference. The FB_CLK signal allows source synchronous timing with rising edge capture for burst control signals and either rising edge capture (SDR mode) or both edge capture (DDR mode) for transmit signal bursts. The FB_CLK signal must have the same frequency and duty cycle as DATA_CLK.

RX_FRAME and TX_FRAME Signals

The device generates an RX_FRAME output signal whenever the receiver outputs valid data. This signal has two modes: level mode (the RX_FRAME signal stays high as long as the data is valid) and pulse mode (the RX_FRAME signal pulses with a 50% duty cycle). Similarly, the BBP must provide a TX_FRAME signal that indicates the beginning of a valid data transmission with a rising edge. Like the RX_FRAME signal, the TX_FRAME signal stays high throughout the burst or it pulses with a 50% duty cycle.

ENABLE STATE MACHINE

The AD9363 transceiver includes an ENSM that allows real-time control over the current state of the device. The device can be placed in several different states during normal operation, including

- Wait—power save, synthesizers disabled
- Sleep—wait with all clocks and the BB PLL disabled
- Tx—Tx signal chain enabled
- Rx—Rx signal chain enabled
- FDD—Tx and Rx signal chains enabled
- Alert—synthesizers enabled

The ENSM has two control modes: SPI control and pin control.

SPI Control Mode

In SPI control mode, the ENSM is controlled asynchronously by writing to SPI registers to advance the current state to the next state. SPI control is considered asynchronous to the DATA_CLK signal because the SPI clock can be derived from a different clock reference and can still function properly. The SPI control ENSM mode is recommended when real-time control of the synthesizers is not necessary. SPI control can be used for real-time control as long as the BBP can perform timed SPI writes accurately.

Pin Control Mode

In pin control mode, the enable functions of the ENABLE pin and the TXNRX pin allow real-time control of the current state. The ENSM allows TDD or FDD operation, depending on the configuration of the corresponding SPI register. The ENABLE and TXNRX pin control mode is recommended if the BBP has extra control outputs that can be controlled in real time, allowing a simple 2-wire interface to control the state of the device. To advance the current state of the ENSM to the next state, drive the enable function of the ENABLE pin by either a pulse (edge detected internally) or a level.

When a pulse is used, it must have a minimum pulse width of one cycle of the FB_CLK signal. In level mode, the ENABLE and TXNRX pins are also edge detected by the AD9363 and must meet the same minimum pulse width requirement of one cycle of the FB_CLK signal.

In FDD mode, the ENABLE and TXNRX pins can be remapped to serve as real-time Rx and Tx data transfer control signals. In this mode, the ENABLE pin assumes the receive on (RXON) function (controls when the Rx path is enabled and disabled), and the TXNRX pin assumes the transmit on (TXON) function (controls when the Tx path is enabled and disabled). The ENSM must be controlled by SPI writes in this mode while the ENABLE and TXNRX pins control all data flow. For more information about RXON and TXON, see the AD9363 reference manual, available from Integrated Wideband RF Transceiver Design Resources.

SPI INTERFACE

The AD9363 uses a serial peripheral interface (SPI) to communicate with the BBP. The SPI can be configured as a 4-wire interface with dedicated receive and transmit ports, or it can be configured as a 3-wire interface with a bidirectional data communication port. This bus allows the BBP to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first six bits set the bus direction and number of bytes to transfer. The next 10 bits set the address where data is to be written. The final eight bits are the data to be transferred to the specified register address (MSB to LSB). The AD9363 also supports an LSB first format that allows the commands to be written in LSB to MSB format. In this mode, the register addresses are incremented for multibyte writes.

Read commands follow a similar format with the exception that the first 16 bits are transferred on the SPI_DI pin, and the final eight bits are read from the AD9363, either on the SPI_DO pin in 4-wire mode or on the SPI_DI pin in 3-wire mode.

CONTROL PINS

Control Outputs (CTRL_OUT7 to CTRL_OUT0)

The AD9363 provides eight simultaneous real-time output signals for use as interrupts to the BBP. These outputs can be configured to output a number of internal settings and measurements that the BBP uses when monitoring trans-ceiver performance in different situations. The control output pointer register selects the information that is output to these pins, and the control output enable register determines which signals are activated for monitoring by the BBP. Signals used for manual gain mode, calibration flags, state machine states, and the ADC output are among the outputs that can be monitored on these pins.

Control Inputs (CTRL_IN3 to CTRL_IN0)

The AD9363 provides four edge detected control input pins. In manual gain mode, the BBP uses these pins to change the gain table index in real time.

GPO PINS (GPO_3 TO GPO_0)

The AD9363 provides four 3.3 V capable general-purpose logic output pins: GPO_3, GPO_2, GPO_1, and GPO_0. These pins control other peripheral devices such as regulators and switches via the AD9363 SPI bus, or they function as slaves for the internal AD9363 state machine.

AUXILIARY CONVERTERS

AUXADC

The AD9363 contains an auxiliary ADC that monitors system functions such as temperature or power output. The converter is 12 bits wide and has an input range of 0.05 V to VDDA1P3_BB – 0.05 V. When enabled, the ADC is free running. SPI reads provide the last value latched at the ADC output. A multiplexer in front of the ADC allows the user to select between the AUXADC input pin and a built-in temperature sensor.

AUXDAC1 and AUXDAC2

The AD9363 contains two identical auxiliary DACs that can provide power amplifier (PA) bias or other system functionality. The auxiliary DACs are 10 bits wide, have an output voltage range of 0.5 V to VDD_GPO – 0.3 V and a current drive of 10 mA, and can be directly controlled by the internal ENSM.

POWERING THE AD9363

The AD9363 must be powered by the following three supplies: the analog supply (VDDx = 1.3 V), the interface supply (VDD_INTERFACE = 1.8 V), and the GPO supply (VDD_GPO = 3.3 V).

For applications requiring optimal noise performance, split and source the 1.3 V analog supply from low noise, low dropout (LDO) regulators. Figure 42 shows the recommended method.

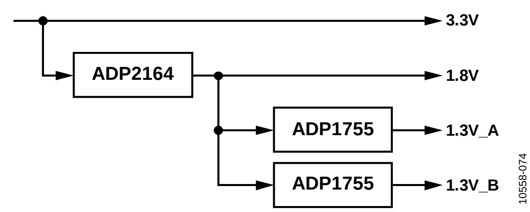


Figure 42. Low Noise Power Solution for the AD9363

For applications where board space is at a premium, and optimal noise performance is not an absolute requirement, provide the 1.3 V analog rail directly from a switcher, and adopt a more integrated power management unit (PMU) approach. Figure 43 shows this approach.

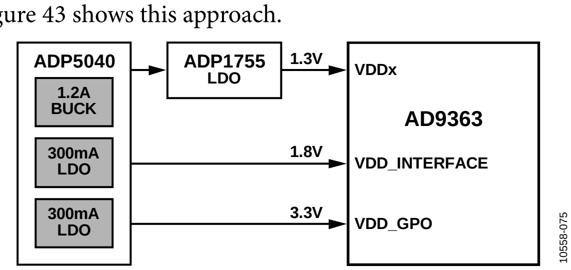


Figure 43. Space Optimized Power Solution for the AD9363

APPLICATIONS INFORMATION

For additional information about how to program the AD9363 device, see the AD9363 reference manual, and for additional information about the AD9363 registers, see the AD9363 register map reference manual, both of which are available by registering at the Integrated Wideband RF Transceiver Design Resources web page and clicking **Download the AD9363 Design File Package**. The register map is provided as a convenient and informational resource about low level operation of the device; however, it is not recommended for creating user software.

Analog Devices, Inc., provides complete drivers for the AD9363 for both bare metal/no operating system (no OS) and Linux operating systems. The AD9361, AD9363, and AD9364 share the same application program interface (API). For the AD9361 drivers, visit the following online locations:

- Linux wiki page
- No OS wiki page

For support for these drivers, visit the following online locations:

- Linux Engineer Zone® page
- No OS Engineer Zone page

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

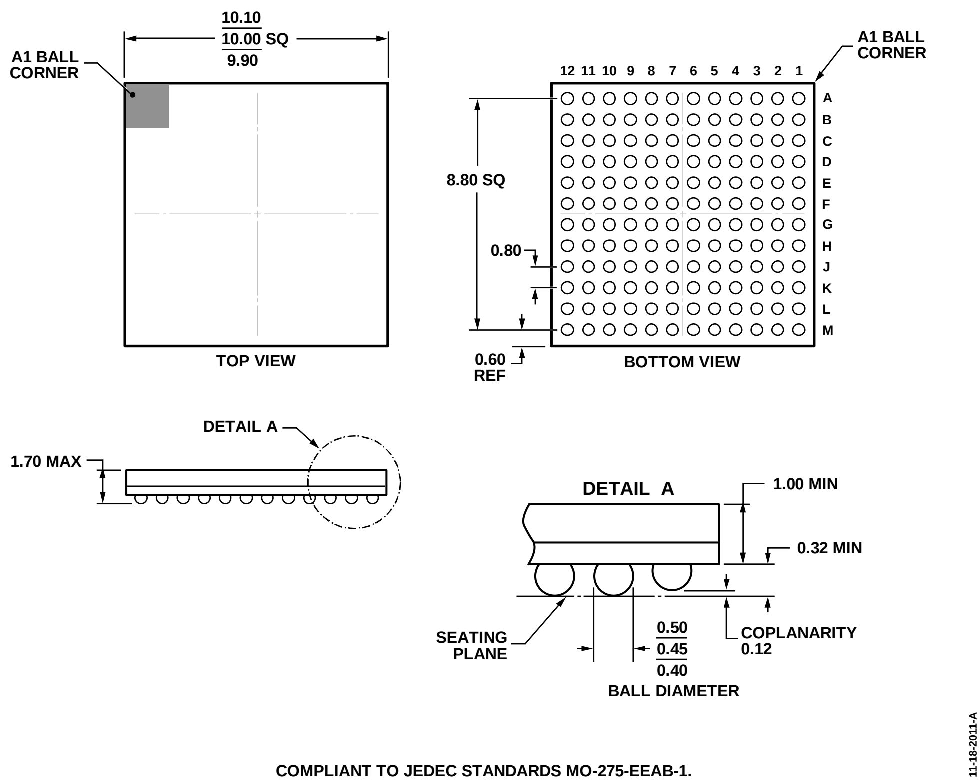


Figure 44. 144-Ball Chip Scale Package Ball Grid Array [CSP_BGA] (BC-144-7) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9363ABCZ	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-7
AD9363ABCZ-REEL	−40°C to +85°C	144-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-144-7
ADRV9363-W/PCBZ		Evaluation Board, 325 MHz to 3800 MHz Matching Circuits	

[1] Z = RoHS Compliant Part.

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