Overview

The MSi2500 converts the analogue baseband outputs from a broadcast silicon tuner to a digital form, performs essential signal processing on those signals and streams them to a PC host over a USB2.0(HS) interface. It is designed for use with the Mirics family of poly-band tuners such as the MSi001 as part of a complete digital TV and radio receiver known as Mirics FlexiTV™.

This approach enables software demodulation on a host CPU, minimizing system cost and maximizing flexibility. The following TV and radio standards can be supported with this approach:

- DVB-T, ISDB-$T_{13\text{-}seg}$, DTMB and ATSC terrestrial TV
- T-DMB, CMMB, DVB-H, ISDB-$T_{1\text{-}seg}$ & ATSC-M/H mobile TV
- AM & FM analog radio
- DAB, DRM & HD digital radio

Designed in a low-cost CMOS process, the MSi2500 integrates: on-chip analog to digital converters, baseband signal processing, microcontroller, embedded memory, power management and high-speed USB2.0 interface.

Applications

- Notebook PCs
- Desktop & media centre PCs
- Net books
- Mobile Internet Devices (“MIDs”)

Features

- Highly integrated device featuring
  - Dual-channel ADC and clock PLL
  - IQ signal processing
  - 8051 microcontroller
  - USB2.0 (HS) interface
  - 24 MHz crystal oscillator and buffer
  - External EEPROM support
  - IR Remote Control support
- Small footprint package
  - 5 x 5 x 0.9 mm 32 pin QFN
- Compliant with all appropriate standards, including:
  - Nordig, EICTA MBRAI, ETSI, ARIB USB2.0(TID=40000840)
- RoHS compliant

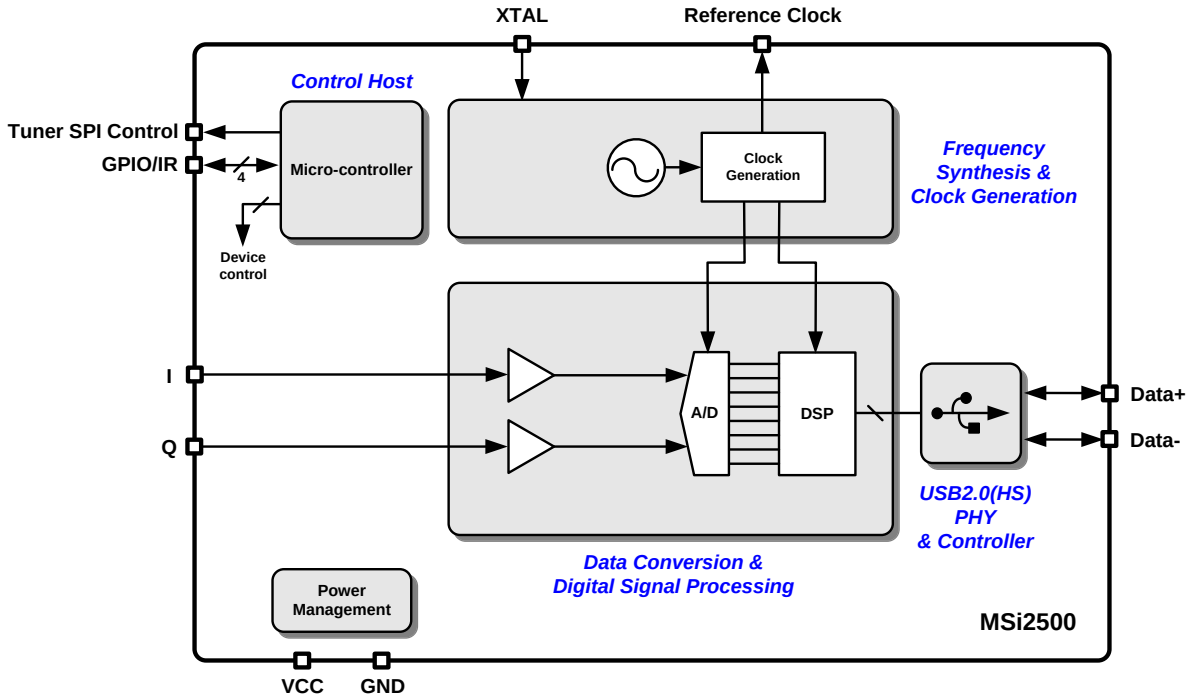


Figure 1: **MSi2500 Top Level Block Diagram**

Contents

1 Functional Block Description

1.1 Dual ADC

The analogue baseband signals from the tuner are digitized by a dual analogue to digital convertor (ADC). The ADC is designed to handle a wide range of broadcast signal bandwidths at low power consumption and provides a resolution of ~10 bits.

1.2 Clock Generation

The ADC sample clock and DSP system clocks are generated by a fully integrated PLL which is configured and tuned appropriately by the Mirics FlexiTV™ software demodulator to meet the specific system requirements of the supported reception modes.

An integrated crystal oscillator is used to generate the required USB 24 MHz reference clock from a 24 MHz crystal. This reference clock is buffered and provided as a CMOS output suitable for use as the tuner reference clock.

1.3 DSP Subsystem

The digital signals from the ADC are conditioned and decimated within the DSP subsystem by a re-configurable digital filter chain that is designed to meet the selectivity requirements of the various systems.

1.4 USB 2.0 (HS)

The USB PHY and controller comply with all USB 2.0 high-speed (480 Mbps) and full-speed (12 Mbps) specifications. To satisfy the bandwidth requirements for IQ data streaming the USB core only ever operates in High-Speed mode. The MSi2500 adopts the USB power management standards to allow a low-power Suspend mode to be supported. The USB endpoint configuration is fixed as “Endpoint 0 and Endpoint 1”, with Endpoint 1 supporting either bulk or isochronous transfers.

1.5 Microcontroller

An 8051 microcontroller, embedded memory, and dedicated control hardware manages the internal housekeeping functions within the MSi2500 while also providing external control of the tuner via a dedicated 3-wire SPI interface. The tuner programming SPI interface operates at 12 MHz. 4 GPIO pins are provided and typical usage models include external EEPROM support and Infra-Red Remote support.

8 kB of embedded RAM provides storage for program code and data, while the default microcode and boot code is stored in a 4 kB on-chip ROM. The default microcode supports full USB operation and all the necessary housekeeping functions required by typical Mirics FlexiTV™ receiver implementation. Alternative microcode can be downloaded either via the USB interface after device boot, or from external EEPROM during device boot.

The default microcode defines the following Vendor and Product ID’s:

Vendor ID: 0x1DF7
Product ID: 0x2500

Alternative VID & PID’s can be supported through use of an external EEPROM.

1.6 Power Management

The MSi2500 operates from a single external 3.3 V supply. An on-chip power management function sub-regulates this 3.3 V input down to multiple 1.8 V core supplies. If required the individual 1.8 V core supplies can be applied externally by overdriving the internal regulators at the output pins provided for LDO decoupling.

1.7 Infra-Red Remote Control Support

The MSi2500 supports the use of an Infra-Red Remote Control by sampling and conditioning a signal from an external IR receiver. This signal is then passed to the host PC over the streaming USB interface for software decode and processing.

2 Device Pin-Out

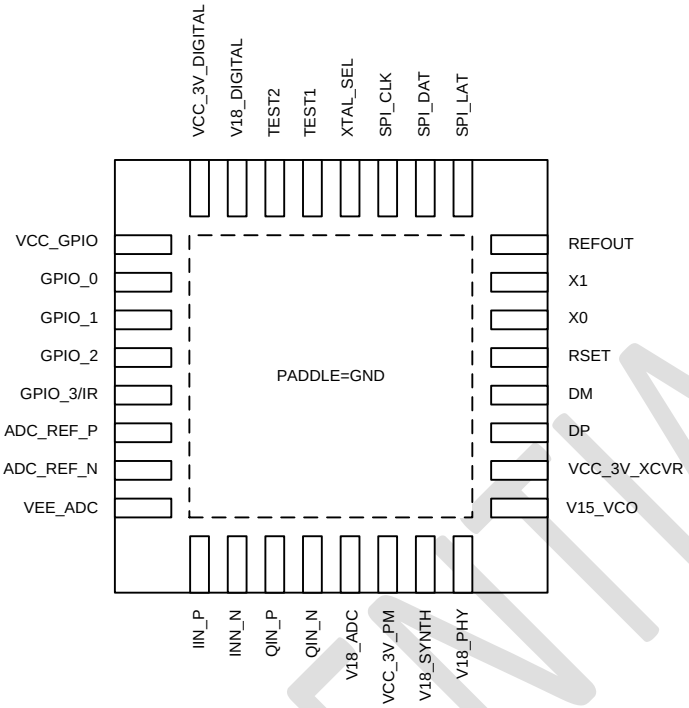


Figure 2: **Pin-Out Diagram (Top View)**

No	Name	Description	No	Name	Description
1	VCC_GPIO	GPIO Supply Regulator Output (1.8 V typ.)	17	V15_VCO	1.5V Regulator Output
2	GPIO_0	GPIO 0	18	VCC_3V_XCVR	3.3 V Supply Input
3	GPIO_1	GPIO 1	19	DP	USB Cable Data P
4	GPIO_2	GPIO 2	20	DM	USB Cable Data M
5	GPIO_3/IR	GPIO 3/Remote control input	21	RSET	Bias Resistor 510R 1%
6	ADC_REF_P	ADC Ref Decoupling	22	X0	24MHz Xtal
7	ADC_REF_N	ADC Ref Decoupling	23	X1	24MHz Xtal
8	VEE_ADC	ADC Ground	24	REFOUT	24MHz Ref Output
9	IIN_P	I Channel ADC input	25	SPI_LAT	Tuner SPI Latch Enable
10	IIN_N	I Channel ADC input	26	SPI_DAT	SPI Data
11	QIN_P	Q Channel ADC input	27	SPI_CLK	SPI Clock
12	QIN_N	Q Channel ADC input	28	XTAL_SEL	Connect to Ground
13	V18_ADC	1.8 V Regulator Output	29	TEST1	Test – Reserved
14	VCC_3V_PM	3.3 V Supply Input	30	TEST2	Test – Reserved
15	V18_SYNTH	1.8 V Regulator Output	31	V18_DIGITAL	1.8 V Regulator Output
16	V18_PHY	1.8 V Regulator Output	32	VCC_3V_DIGITAL	3.3 V Supply Input

Table 1: **Pin-Out**

3 Electrical Specification

3.1 Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below. This device is ESD sensitive, handling and assembly of this device should be at ESD protected workstations.

Parameter	Symbol	Min	Max	Unit
Supply voltage	VCC_3V_x	-0.3	+3.6	V
Storage temperature	Ta	-65	+150	ºC
Case temperature	Tc	-65	+100	ºC
ESD Human Body Model(HBM)	ESD		1000	V
ESD (HBM) USB data lines	ESD_{USB}		2000	V

Table 2: **Absolute Maximum Ratings**

3.2 Recommended Operation

Parameter	Symbol	Min	Typ	Max	Unit
Regulated supply voltage	VCC_3V_x	3.0	3.3	3.6	V
Ambient temperature	T_A	-20	25	85	°C

Table 3: **Recommended Operation**

3.3 Electrical Characteristics

Tc = 25 ºC. VCC_3V_x = 3.3 V unless otherwise stated

Mode	Min	Typ	Max	Unit
DVB-T 8MHz		77		mA
DVB-T 7MHz		74		mA
DVB-T 6MHz {ISDB-T_{13s}}		69		mA
DAB, T-DMB {ISDB-T_{3s}}		46		mA
FM, AM/DRM {ISDB-T_{1s}}		42		mA
Standby[1]		160		µA

Table 4: **Power Consumption**

Tc = 25 ºC. VCC_3V_x = 3.3 V unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low-level input voltage	V_{IL}		0		0.4	V
High-level input voltage	V_{IH}		1.25		V_{GPIO} + 0.3	V
Low-level input current	I_{IL}	V_{IL} = 0.4 V		<0.1		µA
High-level input current	I_{IH}	V_{IH} = 1.8 V		<0.1		µA
Low-level output voltage	V_{OL}	Iout = 2 mA			0.4	V
High-level output voltage	V_{OH}	Iout = -2 mA	1.4	V_{GPIO}		V
High-level output voltage	V_{OHLV}	Iout = -2 mA	1.0	V_{GPIOLV}	V_{GPIOLV} + 0.3	V

Table 5: **GPIO Pins (GPIO_x)**

[1] Excludes current through USB host pull down

Tc = 25 ºC. VCC_3V_x = 3.3 V unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low-level input voltage	V_{IL}		0		0.7	V
High-level input voltage	V_{IH}		1.25		$V_{DIGITAL}$	V
Low-level input current	I_{IL}				1	µA
High-level input current	I_{IH}				1	µA
Low-level output voltage	V_{OL}	I_{OUT} = 0.2 mA			0.4	V
High-level output voltage	V_{OH}	I_{OUT} = -0.2 mA	1.4	$V_{DIGITAL}$		V
Tuner bus frequency	F_{TUN}			12		MHz
EEPROM bus frequency	F_{MEM}			3		MHz
Load capacitance	C_{LOAD}				20	pF

Table 6: **Serial Bus (SPI_x)**

Tc = 25 ºC. VCC_3V_x = 3.3 V unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Overdrive input voltage	V_{XI}		0.4			V
Reference output voltage	V_{REF}		0.8			V
Reference output load	C_{LOADX}				20	pF
Oscillator output load (X1)	C_{X1}				50	pF

Table 7: **Reference Clock**

Tc = 25 ºC. VCC_3V_x = 3.3 V unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC_GPIO	V_{GPIO}	I_{OUT} = 5 mA	1.75	1.8		V
VCC_GPIO_LV_Mode	V_{GPIO_LV}	I_{OUT} = 0.3 mA	1.15	1.2		V
V18_DIGITAL	$V_{DIGITAL}$	I_{OUT} = 0.3 mA	1.75	1.8		V
V18_SYNTH	V_{SYNTH}	I_{OUT} = 0.3 mA	1.5	1.8		V
V18_SYNTH_OFF	$V_{SUSPEND}$	Suspend state			0.2	V

Table 8: **Regulators**

4 Application Circuit Guidelines

4.1 Crystal Oscillator

The MSi2500 has an on-chip crystal oscillator circuit which operates with a 24 MHz crystal attached between the X0 and X1 pins. The XTAL_SEL should be pulled to ground to bypass the internal clock divider.

The crystal manufacturer's specified load capacitors should connected as shown in Figure 3:. Oscillator start-up time with this configuration is typically less than 200 µs. Alternatively an external reference can be AC coupled to X0 with X1 being left open circuit.

- Initial frequency Tolerance ± 20ppm
- Frequency tolerance ± 30ppm over the desired temperature range.

The MSi2500 can support load capacitances up to 15 pF. Any values in excess of this can cause a reduction in the amplitude of the oscillator which could stop correct operation of the MSi2500. In order to calculate the value of the load capacitors C_{LOAD0} and C_{LOAD1} the following formula can be used.

$$Crystal\ Load\ Capacitance = [C_{LOAD0} + CX0]\ x\ [C_{LOAD1} + CX1] \div [C_{LOAD0} + CX0 + C_{LOAD1} + CX1]$$

In this instance CX0 and CX1 reflects the capacitance presented by the internal oscillator and any stray PCB capacitance. Nominally this tends to be around 2 to 3 pF but will depend on the board layout. Also note that the load capacitors are normally selected to be the same value. So the equation simplifies to such that the load capacitors are twice the crystal load capacitance minus any stray capacitance.

The load capacitance effectively limits the voltage swing at X0 which degrades phase noise of the REFOUT output. This in turn degrades the RF phase noise of the tuner and system performance. A good RF Swing at X0 should be > 0.8 V peak to peak.

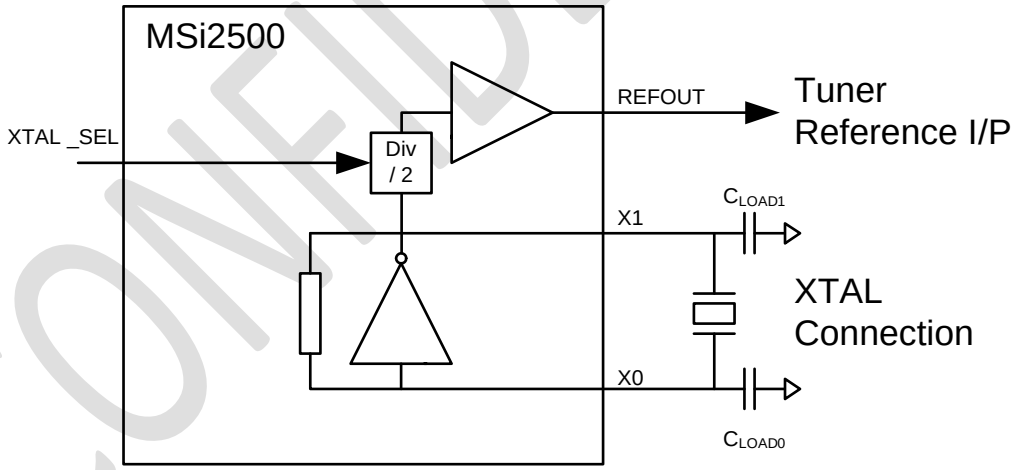


Figure 3: **Crystal Oscillator Configuration**

4.2 External EEPROM

An external serial EEPROM can be used to either provide support for customer specific USB VID & PID's or to allow use of an alternative 8051 microcode. The EEPROM should be interfaced to the MSi2500 via the SPI and GPIO interface as shown below:

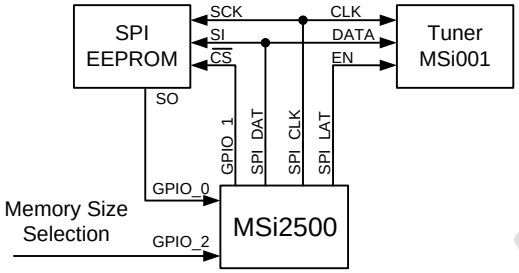


Figure 4: **Memory and Tuner Interface**

In this configuration the SPI_CLK and SPI_DAT lines are used for communication with the EEPROM during device boot. GPIO_0 receives output data from the EEPROM, whereas GPIO_1 controls the EEPROM chip-select line during the boot sequence. A pull-up or pull-down resistor should be fitted on GPIO_2 to specify which EEPROM size is being used in the application circuit. This allows support for both 9 bit and 16 bit addressed serial SPI EEPROM's. To operate with a 9-bit addressed EEPROM GPIO_2 should be tied to ground, to operate with a 16-bit addressed device it should be tied to 1.8 V.

During device boot the internal control logic reads back the first byte of data from the EEPROM over the SPI port. If 0xB4 is found then the VID, PID and Device Release information in the EEPROM will replace the default values stored within the MSi2500 ROM and these customer specific values will be assumed during USB enumeration. If 0xD2 is found then an alternative microcode program will be loaded from the EEPROM and used during subsequent operation. If no EEPROM is fitted then GPIO_0 should be fitted with a pull-down, this will be detected during the boot sequence and the default microcode and ID's will be used from the internal ROM.

4.3 IR Remote Control Support

An external IR receiver IC can be interfaced to the MSi2500 via the GPIO_3 pin. Within the MSi2500 the input signal stream is sampled internally, the duration and sense of each pulse is detected and converted to an appropriate byte stream. This byte stream is then inserted in the USB packet headers and streamed to the host PC together with the digital IQ receiver data. The IR byte stream can then be converted to RLC format by the host PC.

The incoming signal on GPIO_3 will be sampled based on a 50 µs period, and the generated byte stream will be coded as follows:

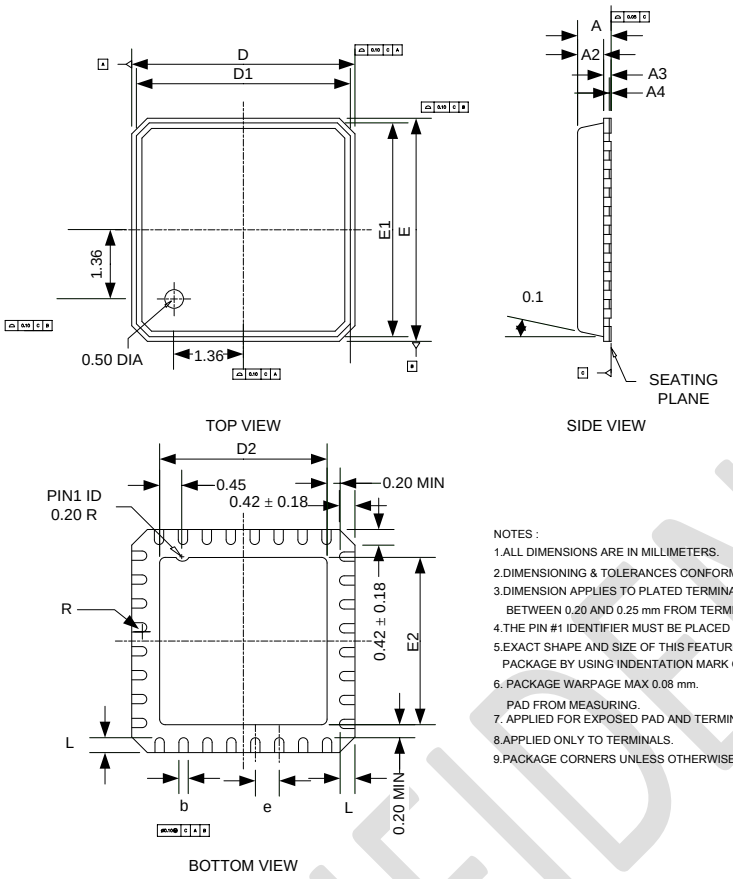
- If the incoming pulse on GPIO_3 is low the byte-MSB is set, else the byte-MSB is cleared
- The pulse duration (measured in the number of 50 µs periods) is measured

For example:

- High pulse lasting 2650 µs → 0x35 [MSB = 0, count = 0x35 = 53 x 50 µs = 2650 µs]
- Low pulse lasting 850 µs → 0x91 [MSB = 1, count = 0x11 = 17 x 50 µs = 850 µs]

5 Ordering and Package Information

5.1 Package Drawing



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	0.00	0.01	0.05	0.00	0.0004	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.18	0.23	0.30	0.007	0.009	0.012
D	5.00 bsc			0.197 bsc		
D1	4.75 bsc			0.187 bsc		
D2	3.55	3.7	3.85	0.14	0.146	0.152
E	5.00 bsc			0.197 bsc		
E1	4.75 bsc			0.187 bsc		
E2	3.55	3.7	3.85	0.140	0.146	0.152
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.50 bsc			0.020 bsc		
θ1	0°	---	12°	0°	---	12°
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
3.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINALTIP.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL. PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. PACKAGE WARPAGE MAX 0.08 mm. PAD FROM MEASURING.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED
8.APPLIED ONLY TO TERMINALS.
9.PACKAGE CORNERS UNLESS OTHERWISE SPECIFIED ARE 0.175±0.025mm

5.2 Marking information

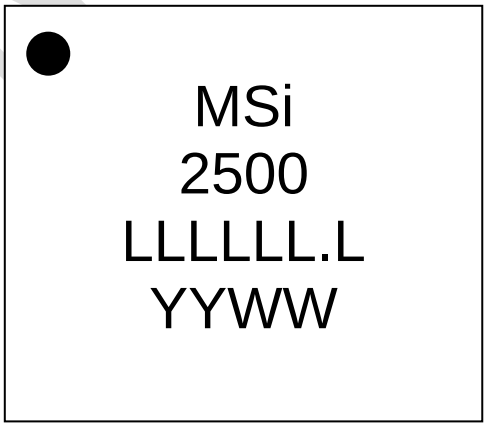


Figure 5: **Package Marking**

LLLLLL.L refers to the wafer lot number and YYWW is the mold week.

5.3 Ordering Information

Ordering code format

MSiXXXX-PPP-T-FF

XXXX	Part Number		
PPP	Package Type		
		Q32	5 x 5 mm QFN 32 pin
T	Temperature Range		
		C	Commercial (-20 to +85 °C)
FF	Finishing Form		
		DS	Dry pack Trays
		DT	Dry pack tape and reel
		NS	Non-Dry pack Trays
		NT	Non- Dry pack tape and reel

Code	Description
MSi2500-Q32-C-DS	MSi2500 Dry pack trays
MSi2500-Q32-C-DT	MSi2500 Dry pack tape and reel

Table 9: **Ordering Information**

For more information contact:

Mirics Semiconductor Inc
Oakmere, Barley Way
Ancells Business Park
Fleet, Hampshire
GU51 2UT UK

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