6.5 V, 4 A, High Efficiency, Step-Down, DC-to-DC Regulator

Data Sheet **ADP2164**

FEATURES

- 4 A continuous output current
- 43 mΩ and 29 mΩ integrated FET
- ±1.5% output accuracy
- Input voltage range: 2.7 V to 6.5 V
- Output voltage: 0.6 V to V_{IN}
- Switching frequency
  - Fixed frequency: 600 kHz or 1.2 MHz
  - Adjustable frequency: 500 kHz to 1.4 MHz
- Synchronizable from 500 kHz to 1.4 MHz
- Selectable synchronize phase shift: 0° or 180°
- Current mode architecture
- Precision enable input
- Power-good output
- Voltage tracking input
- Integrated soft start
- Internal compensation
- Starts up into a precharged output
- UVLO, OVP, OCP, and thermal shutdown
- Available in 16-lead, 4 mm × 4 mm LFCSP package
- Supported by ADIsimPower™ design tool

APPLICATIONS

- Point-of-load conversion
- Communications and networking equipment
- Industrial and instrumentation
- Consumer electronics

TYPICAL APPLICATIONS CIRCUIT

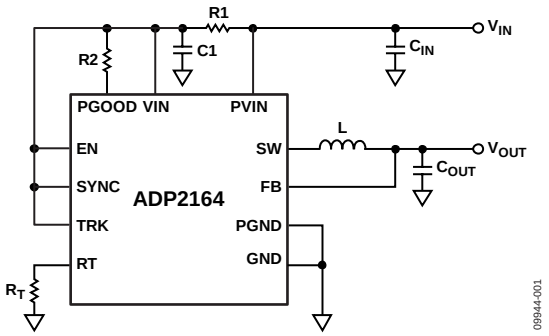

Figure 1.

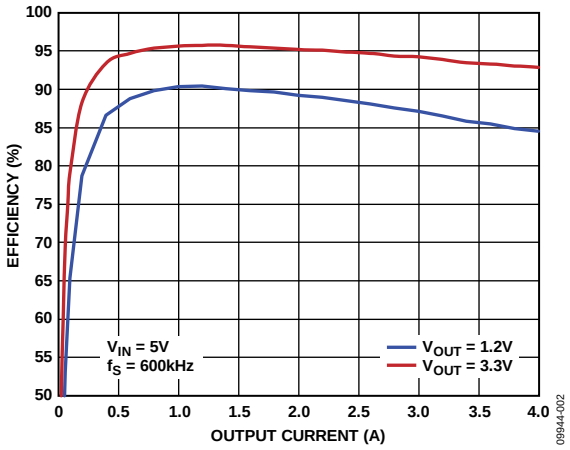

Figure 2. Efficiency vs. Output Current

GENERAL DESCRIPTION

The ADP2164 is a 4 A, synchronous, step-down, dc-to-dc regulator in a compact 4 mm × 4 mm LFCSP package. The regulator uses a current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient response.

The input voltage range of the ADP2164 is 2.7 V to 6.5 V. The output voltage of the ADP2164 is adjustable from 0.6 V to the input voltage (V_{IN}). The ADP2164 is also available in six preset output voltage options: 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, and 1.0 V.

The ADP2164 integrates a pair of low on-resistance P-channel and N-channel internal MOSFETs to maximize efficiency and minimize external component count. The 100% duty cycle operation allows low dropout voltage at 4 A output current.

The high, 1.2 MHz PWM switching frequency allows the use of small external components, and the SYNC input enables multiple ICs to synchronize out of phase to reduce ripple and eliminate beat frequencies.

Other key features of the ADP2164 include undervoltage lockout (UVLO), integrated soft start to limit inrush current at startup, overvoltage protection (OVP), overcurrent protection (OCP), and thermal shutdown.

Rev. C

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REVISION HISTORY

6/2018—Rev. B to Rev. C

Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

8/2017—Rev. A to Rev. B

Changed CP-16-26 to CP-16-17 ... Throughout
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

6/2012—Rev. 0 to Rev. A

Changes to Features Section ... 1
Added ADIsimPower Design Tool Section ... 16

12/2011—Revision 0: Initial Version

SPECIFICATIONS

VIN = PVIN = 3.3 V, EN high, SYNC high, T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VIN AND PVIN PINS						
VIN Voltage Range	VIN		2.7		6.5	V
PVIN Voltage Range	PVIN		2.7		6.5	V
Quiescent Current	I_{VIN}	No switching		895	1100	µA
Shutdown Current	I_{SHDN}	VIN = PVIN = 6.5 V, EN = GND		9	12	µA
VIN Undervoltage Lockout Threshold	UVLO	VIN rising		2.6	2.7	V
		VIN falling	2.4	2.5		V
OUTPUT CHARACTERISTICS		Specified by the circuit in Figure 42				
Load Regulation		I_O = 0 A to 4 A		0.05		%/A
Line Regulation		I_O = 2 A		0.05		%/V
FB PIN						
FB Regulation Voltage	V_{FB}	T_J = −40°C to +125°C	0.591	0.6	0.609	V
FB Bias Current	I_{FB}			0.01	0.1	µA
SW PIN						
High-Side On Resistance[1]		VIN = PVIN = 3.3 V, I_{SW} = 500 mA	35	52	70	mΩ
		VIN = PVIN = 5 V, I_{SW} = 500 mA	30	43	55	mΩ
Low-Side On Resistance[1]		VIN = PVIN = 3.3 V, I_{SW} = 500 mA	24	32	40	mΩ
		VIN = PVIN = 5 V, I_{SW} = 500 mA	20	29	35	mΩ
SW Peak Current Limit		High-side switch, PVIN = 3.3 V	5	6.2	7.4	A
SW Maximum Duty Cycle		Full frequency			100	%
SW Minimum On Time[2]		Full frequency		100		ns
TRK PIN						
TRK Input Voltage Range			0		600	mV
TRK to FB Offset Voltage		TRK = 0 mV to 500 mV	−15		+15	mV
TRK Input Bias Current					100	nA
FREQUENCY						
Switching Frequency	f_S	RT = VIN	1.08	1.2	1.32	MHz
		RT = GND	540	600	660	kHz
		RT = 91 kΩ	480	600	720	kHz
Switching Frequency Range			500		1400	kHz
RT Pin Input High Voltage			1.2			V
RT Pin Input Low Voltage					0.45	V
SYNC PIN						
Synchronization Range			0.5		1.4	MHz
Minimum Pulse Width			100			ns
Minimum Off Time			100			ns
Input High Voltage			1.2			V
Input Low Voltage					0.4	V
PGOOD PIN						
Power-Good Range		FB rising threshold	105	110	115	%
		FB rising hysteresis		2.5		%
		FB falling threshold	85	90	95	%
		FB falling hysteresis		2.5		%
Power-Good Deglitch Time		From FB to PGOOD		16		Clock cycles
Power-Good Leakage Current		V_{PGOOD} = 5 V		0.1	1	µA
Power-Good Output Low Voltage		I_{PGOOD} = 1 mA		170	220	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INTEGRATED SOFT START						
Soft Start Time		All switching frequencies		2048		Clock cycles
EN PIN						
EN Input Rising Threshold			1.12	1.2	1.28	V
EN Input Hysteresis				100		mV
EN Pull-Down Resistor				1		MΩ
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		T_J increasing		140		°C
Thermal Shutdown Hysteresis				15		°C

[1] Pin-to-pin measurements.
[2] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN, VIN, SW	−0.3 V to +7 V
FB, SYNC, TRK, RT, EN, PGOOD	−0.3 V to +7 V
PGND to GND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is measured using natural convection on a JEDEC 4-layer board. The exposed pad is soldered to the printed circuit board with thermal vias.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP	38.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

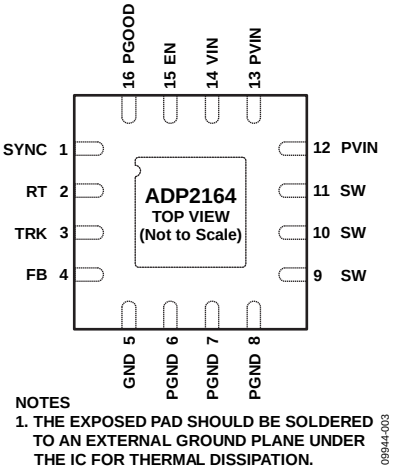


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SYNC	Synchronization Input. To synchronize the switching frequency to an external clock, connect this pin to an external clock with a frequency of 500 kHz to 1.4 MHz (see the Oscillator and Synchronization section for more information).
2	RT	Frequency Setting. To select a switching frequency of 600 kHz, connect this pin to GND; to select a switching frequency of 1.2 MHz, connect this pin to VIN. To program the frequency from 500 kHz to 1.4 MHz, connect a resistor from this pin to GND (see the Oscillator and Synchronization section for more information).
3	TRK	Tracking Input. To track a master voltage, connect the TRK pin to a voltage divider from the master voltage. If the tracking function is not used, connect the TRK pin to VIN. For more information, see the Voltage Tracking section.
4	FB	Feedback Voltage Sense Input. Connect this pin to a resistor divider from V_{OUT}. For the preset output version, connect this pin directly to V_{OUT}.
5	GND	Analog Ground. Connect to the ground plane.
6, 7, 8	PGND	Power Ground. Connect to the ground plane and to the output return side of the output capacitor.
9, 10, 11	SW	Switch Node Output. Connect to the output inductor.
12, 13	PVIN	Power Input Pin. Connect this pin to the input power source. Connect a bypass capacitor between this pin and PGND.
14	VIN	Bias Voltage Input Pin. Connect a bypass capacitor between this pin and GND; connect a small (10 Ω) resistor between this pin and PVIN.
15	EN	Precision Enable Pin. The external resistor divider can be used to set the turn-on threshold. To enable the part automatically, connect the EN pin to VIN. This pin has a 1 MΩ pull-down resistor to GND.
16	PGOOD	Power-Good Output (Open Drain). Connect this pin to a resistor from any pull-up voltage lower than 6.5 V.
17 (EPAD)	Exposed Pad	The exposed pad should be soldered to an external ground plane under the IC for thermal dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, V_{IN} = 5 V, V_{OUT} = 1.2 V, L = 1 µH, C_{IN} = 47 µF, C_{OUT} = 100 µF, unless otherwise noted.

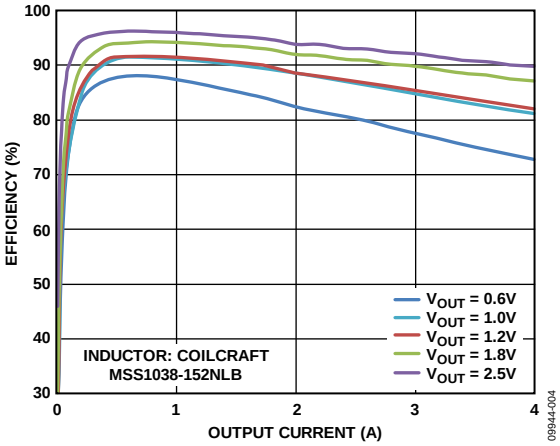


Figure 4. Efficiency vs. Output Current, V_{IN} = 3.3 V, f_S = 600 kHz

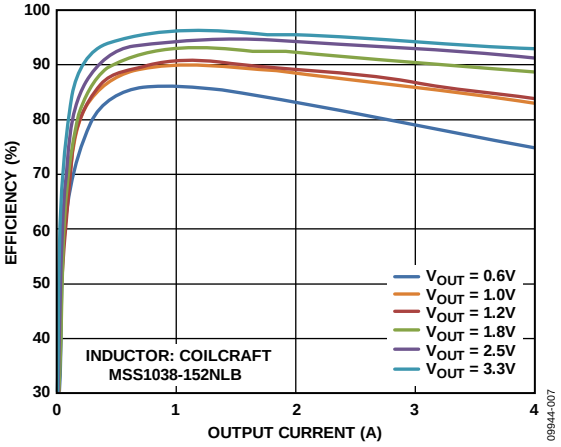


Figure 7. Efficiency vs. Output Current, V_{IN} = 5 V, f_S = 600 kHz

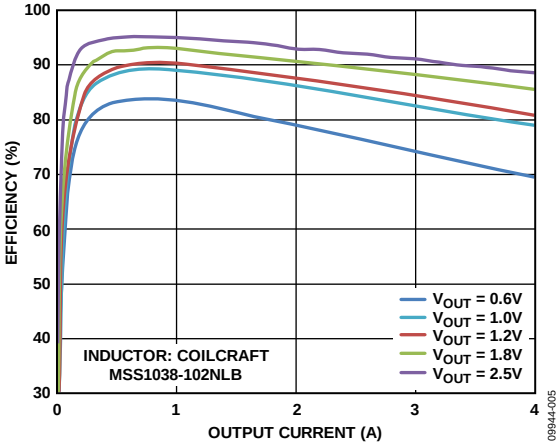


Figure 5. Efficiency vs. Output Current, V_{IN} = 3.3 V, f_S = 1.2 MHz

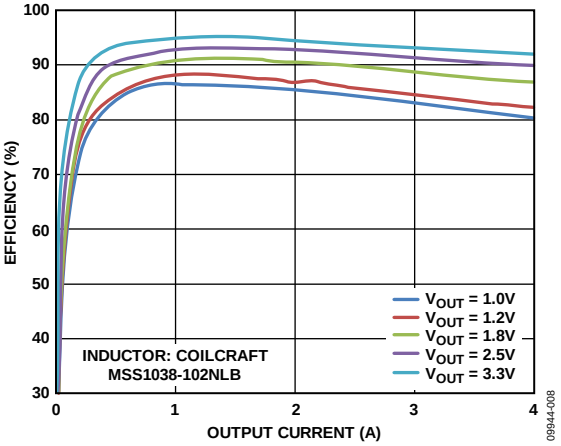


Figure 8. Efficiency vs. Output Current, V_{IN} = 5 V, f_S = 1.2 MHz

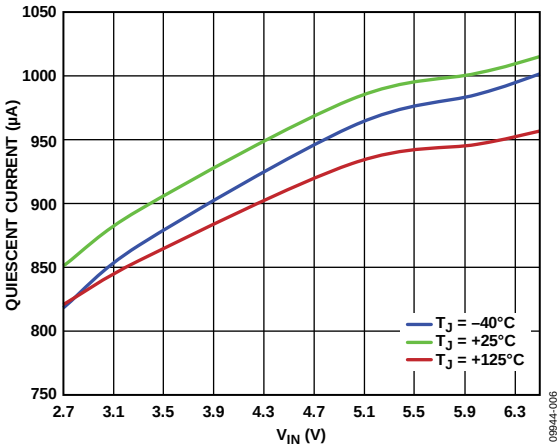


Figure 6. Quiescent Current vs. V_{IN} (No Switching)

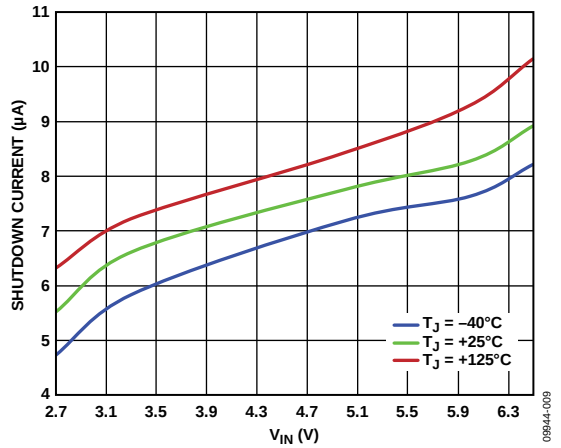


Figure 9. Shutdown Current vs. V_{IN}

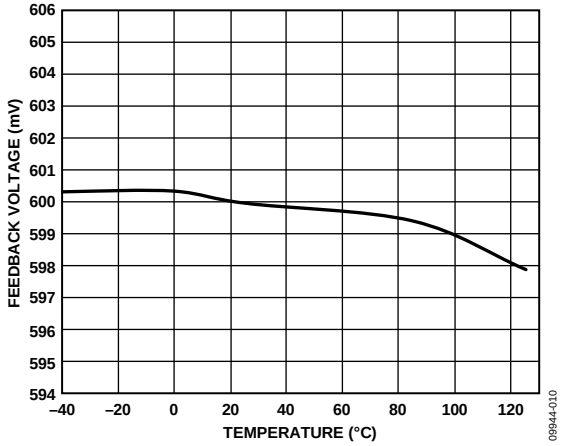


Figure 10. Feedback Voltage vs. Temperature, V_{IN} = 3.3 V

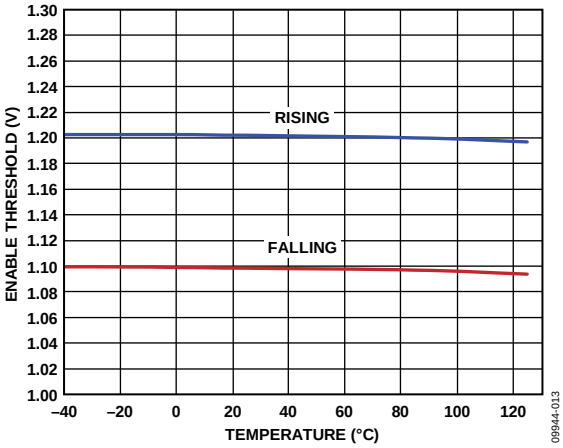


Figure 13. EN Threshold vs. Temperature

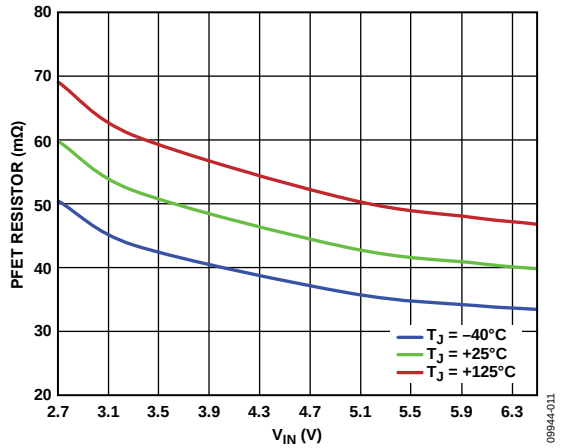


Figure 11. PFET Resistor vs. V_{IN} (Pin-to-Pin Measurements)

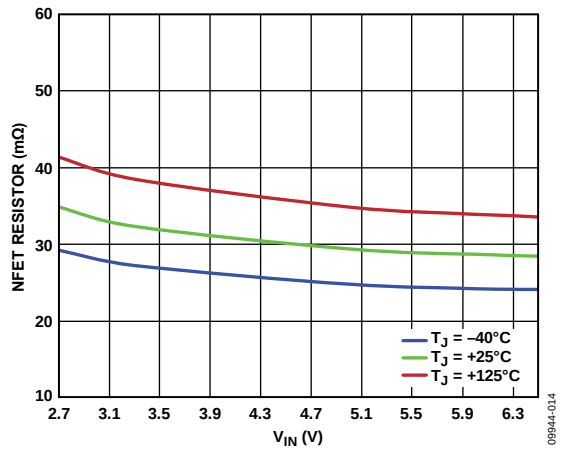


Figure 14. NFET Resistor vs. V_{IN} (Pin-to-Pin Measurements)

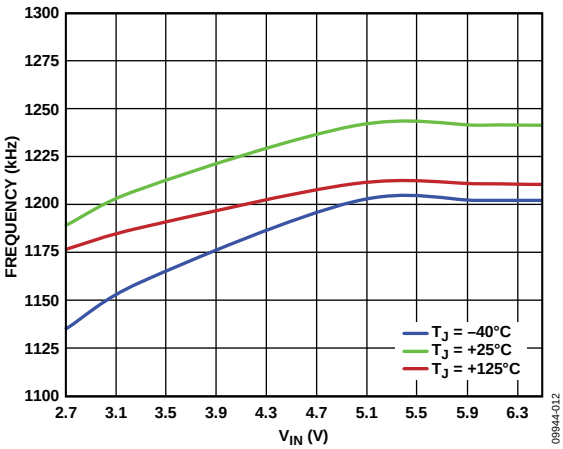


Figure 12. Switching Frequency vs. V_{IN}, f_S = 1.2 MHz (RT = VIN)

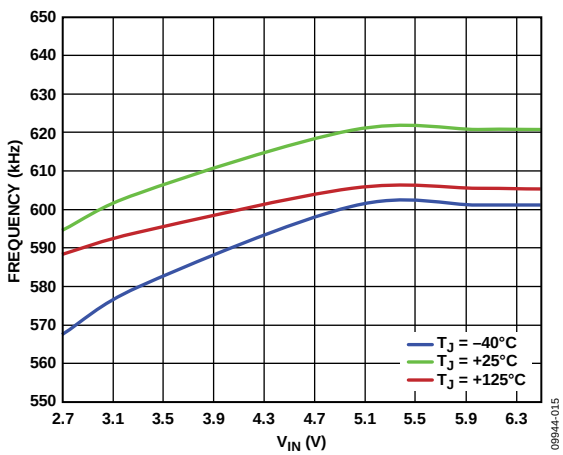


Figure 15. Switching Frequency vs. V_{IN}, f_S = 600 kHz (RT = GND)

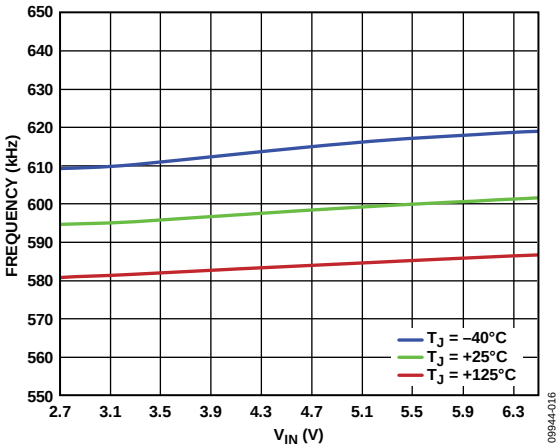


Figure 16. Switching Frequency vs. V_{IN}, f_S = 600 kHz (RT = 91 kΩ)

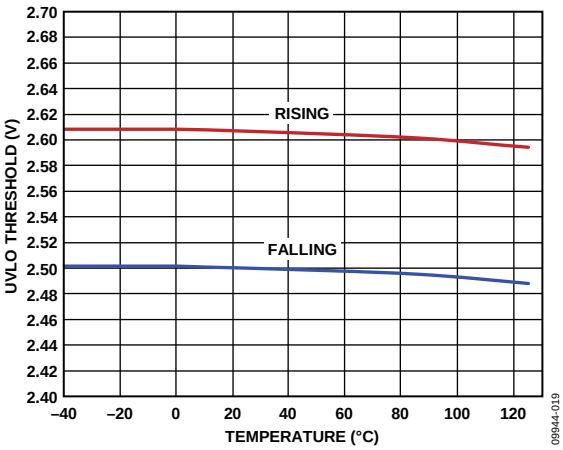


Figure 19. UVLO Threshold vs. Temperature, V_{IN} = 3.3 V

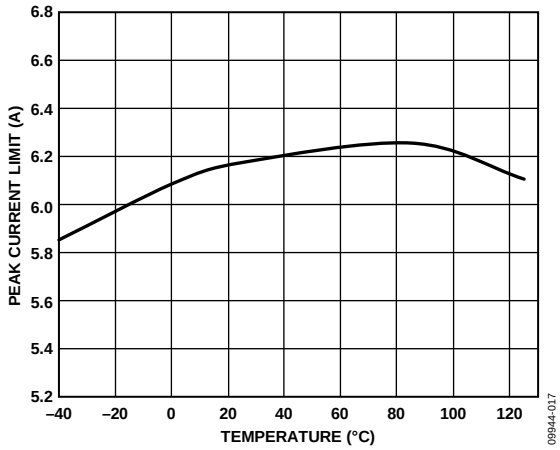


Figure 17. Peak Current Limit vs. Temperature, V_{IN} = 3.3 V

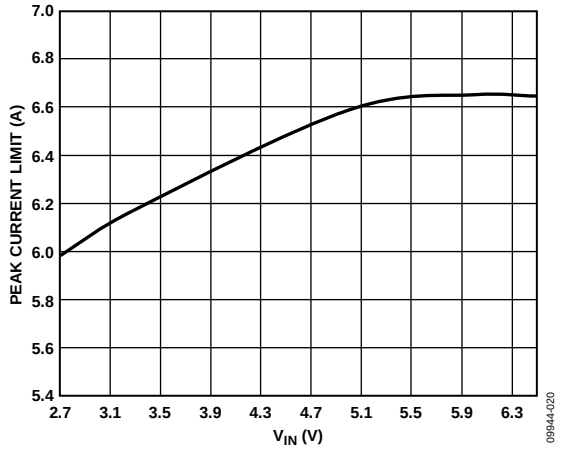


Figure 20. Peak Current Limit vs. V_{IN}, T_J = 25°C

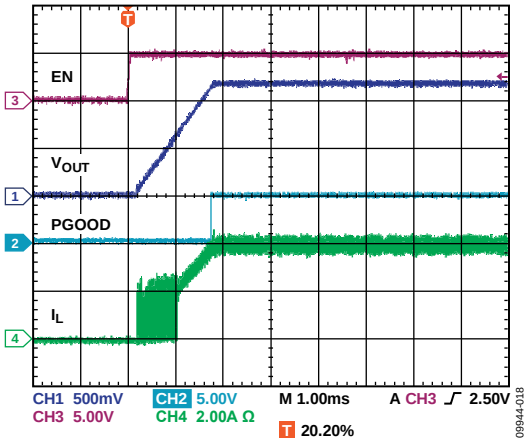


Figure 18. Soft Start with Full Load, V_{IN} = 5 V, V_{OUT} = 1.2 V, f_S = 1.2 MHz

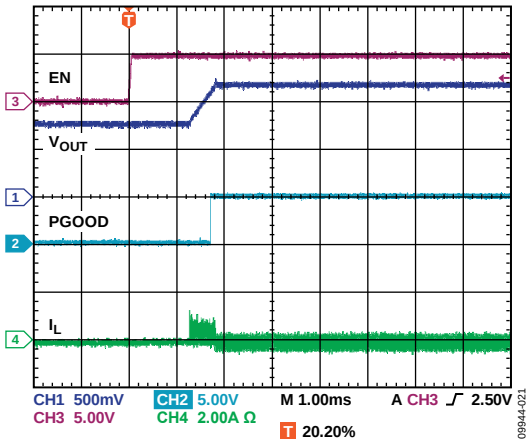


Figure 21. Soft Start with Precharged Output Voltage, V_{IN} = 5 V, f_S = 1.2 MHz

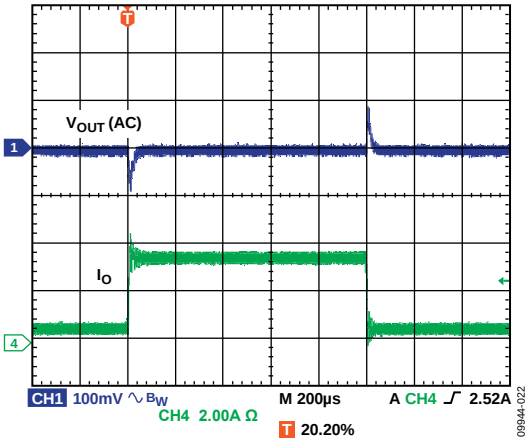


Figure 22. Load Transient, 0.5 A to 3.5 A Load Step, V_{IN} = 5 V, V_{OUT} = 1.2 V, f_S = 1.2 MHz

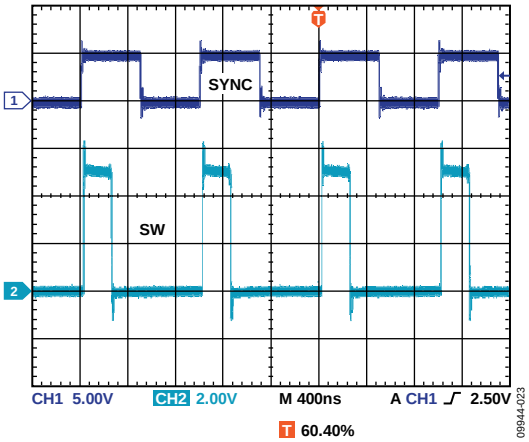


Figure 23. ADP2164 Synchronized to 1 MHz, in Phase

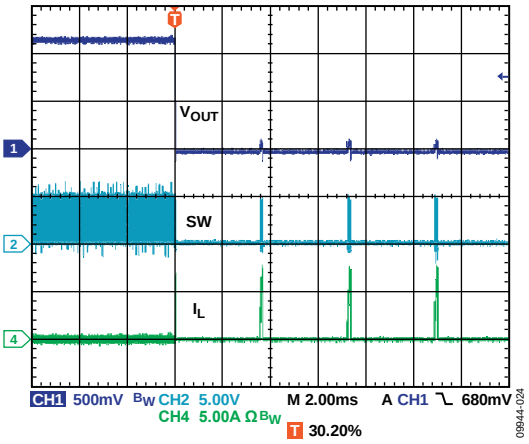


Figure 24. Output Short

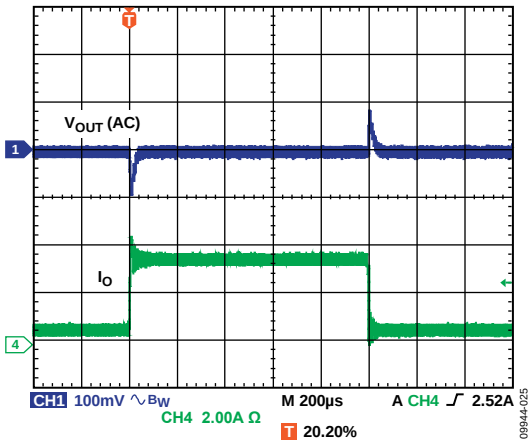


Figure 25. Load Transient, 0.5 A to 3.5 A Load Step, V_{IN} = 5 V, V_{OUT} = 1.2 V, f_S = 600 kHz

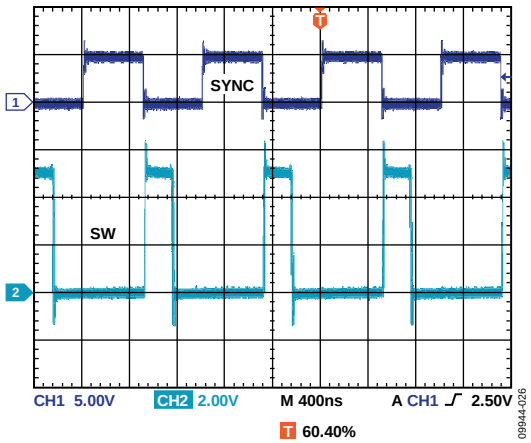


Figure 26. ADP2164 Synchronized to 1 MHz, 180° out of Phase

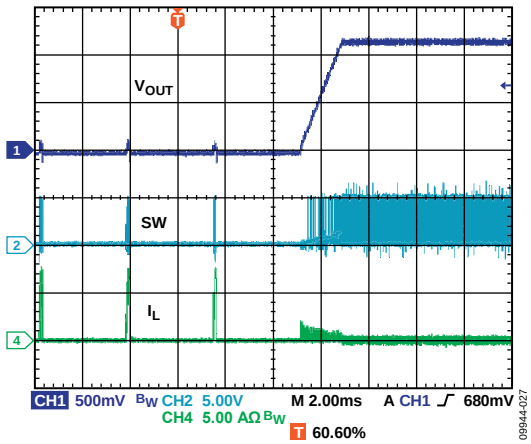


Figure 27. Output Short Recovery

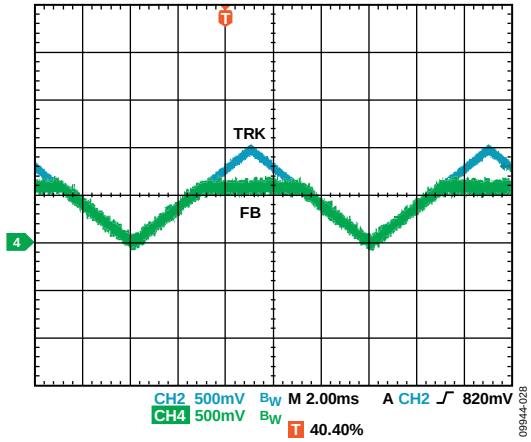


Figure 28. Tracking Function

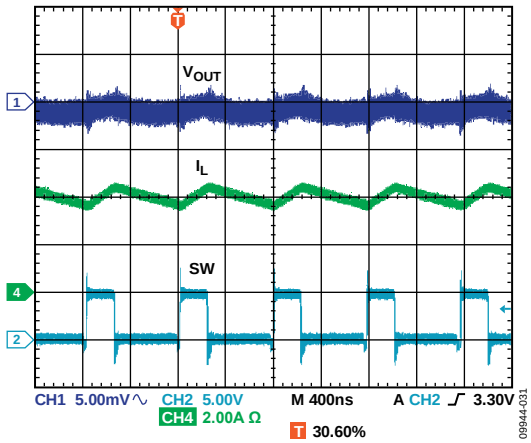


Figure 31. Steady Waveform, V_{IN} = 5 V, V_{OUT} = 1.2 V, f_S = 1.2 MHz

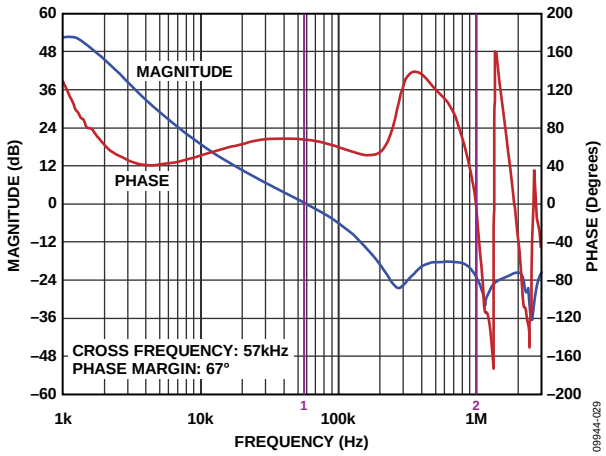


Figure 29. Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.0 V, I_O = 4 A, f_S = 1.2 MHz, L = 0.68 µH, C_{OUT} = 2 × 100 µF

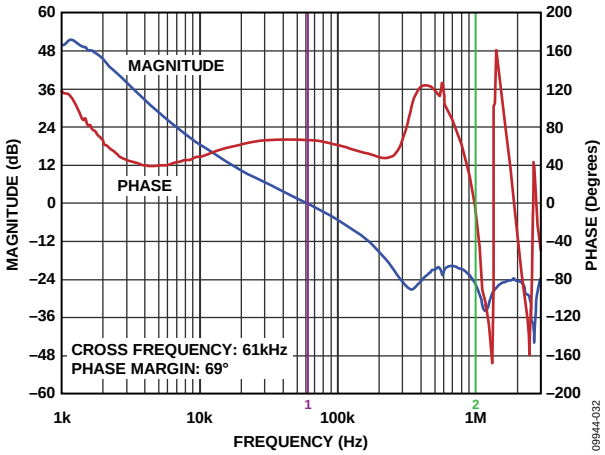


Figure 32. Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.2 V, I_O = 4 A, f_S = 1.2 MHz, L = 0.68 µH, C_{OUT} = 47 µF + 100 µF

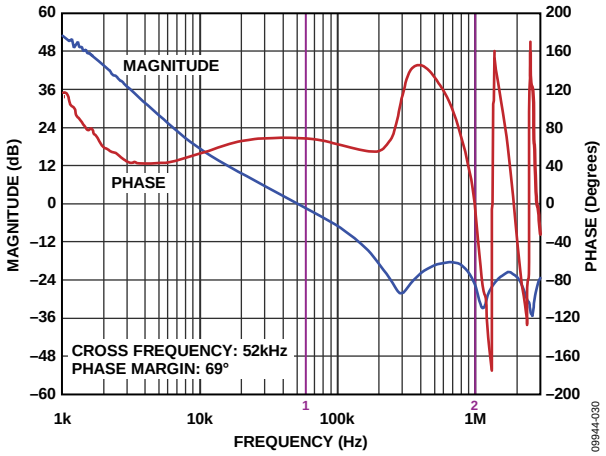


Figure 30. Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.5 V, I_O = 4 A, f_S = 1.2 MHz, L = 1 µH, C_{OUT} = 47 µF + 100 µF

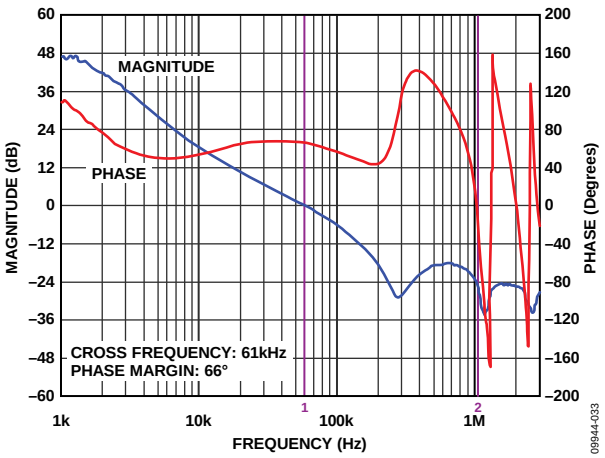


Figure 33. Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.8 V, I_O = 4 A, f_S = 1.2 MHz, L = 1 µH, C_{OUT} = 100 µF

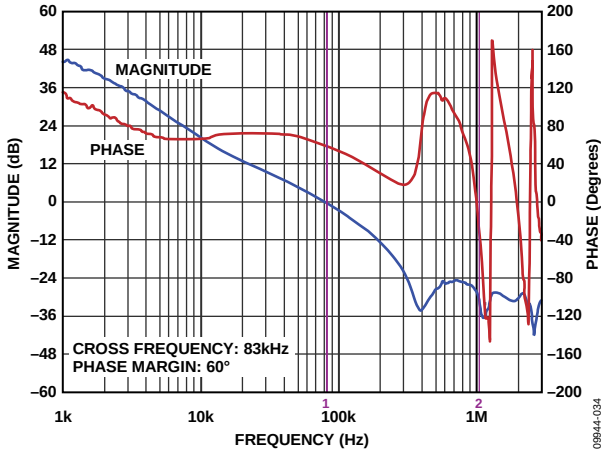


Figure 34. Bode Plot at V_{IN} = 5 V, V_{OUT} = 2.5 V, I_O = 4 A, f_S = 1.2 MHz, L = 1 µH, C_{OUT} = 47 µF

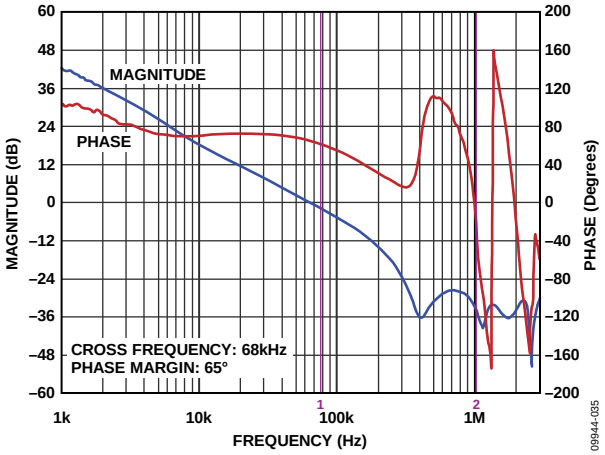


Figure 35. Bode Plot at V_{IN} = 5 V, V_{OUT} = 3.3 V, I_O = 4 A, f_S = 1.2 MHz, L = 1 µH, C_{OUT} = 47 µF

FUNCTIONAL BLOCK DIAGRAM

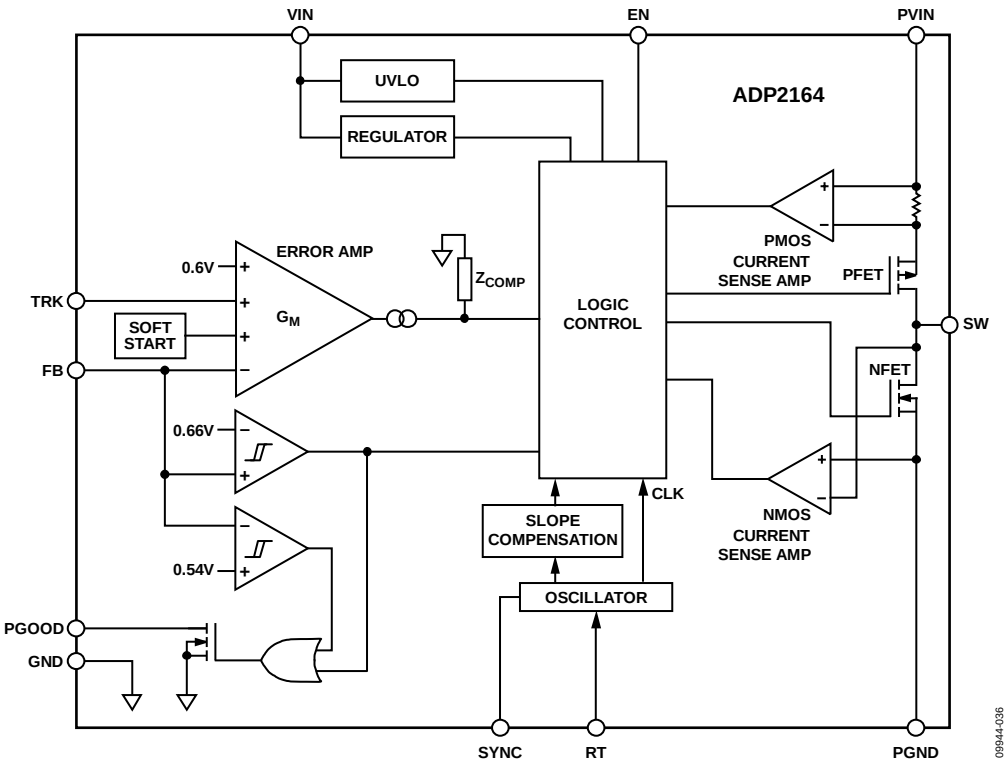


Figure 36. Functional Block Diagram

THEORY OF OPERATION

The ADP2164 is a step-down dc-to-dc regulator that uses a fixed-frequency, peak current mode architecture with an integrated high-side switch and low-side synchronous rectifier. The high switching frequency and tiny, 16-lead, 4 mm × 4 mm LFCSP package provide a small, step-down dc-to-dc regulator solution. The integrated high-side switch (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET) yield high efficiency.

The ADP2164 operates with an input voltage from 2.7 V to 6.5 V and regulates the output voltage down to 0.6 V. The ADP2164 is also available with preset output voltage options of 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, and 1.0 V.

CONTROL SCHEME

The ADP2164 uses a fixed-frequency, peak current mode PWM control architecture. At the start of each oscillator cycle, the P-channel MOSFET switch is turned on, placing a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current level, turns off the P-channel MOSFET switch, and turns on the N-channel MOSFET synchronous rectifier. This action places a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle.

The peak inductor current level is set by the compensation (COMP) voltage. The COMP voltage is the output of a transconductance error amplifier that compares the feedback voltage with an internal 0.6 V reference (see Figure 36).

SLOPE COMPENSATION

To prevent subharmonic oscillations, slope compensation stabilizes the internal current control loop of the ADP2164 when the part operates at or beyond a 50% duty cycle. Slope compensation is implemented by summing an artificial voltage ramp with the current sense signal during the on time of the P-channel MOSFET switch. This voltage ramp depends on the output voltage. When operating at high output voltages, slope compensation increases. The slope compensation ramp value determines the minimum inductor value that can be used to prevent subharmonic oscillations.

PRECISION ENABLE/SHUTDOWN

The EN pin is a precision analog input that enables the device when the voltage exceeds 1.2 V (typical); this pin has 100 mV hysteresis. When the enable voltage falls below 1.1 V (typical), the part turns off. To force the ADP2164 to start automatically when input power is applied, connect the EN pin to the VIN pin.

When the ADP2164 is shut down, the soft start capacitor is discharged. This causes a new soft start cycle to begin when the part is reenabled.

An internal pull-down resistor (1 MΩ) prevents accidental enabling of the part if the EN input is left floating.

INTEGRATED SOFT START

The ADP2164 has integrated soft start circuitry to limit the output voltage rise time and reduce inrush current at startup. The soft start time is set at 2048 clock cycles.

If the output voltage is precharged before the part is turned on, the ADP2164 prevents a reverse inductor current (which would discharge the output capacitor) until the soft start voltage exceeds the voltage on the FB pin.

OSCILLATOR AND SYNCHRONIZATION

The ADP2164 switching frequency is controlled by the RT pin. If the RT pin is connected to GND, the switching frequency is set to 600 kHz. If the RT pin is connected to VIN, the switching frequency is set to 1.2 MHz.

Connecting a resistor from RT to GND allows programming of the switching frequency from 500 kHz to 1.4 MHz. Use the following equation to set the switching frequency:

$$RT\,(\text{k}\Omega) = \frac{54{,}000}{f_S\,(\text{kHz})}$$

Figure 37 shows the typical relationship between the switching frequency and the RT resistor.

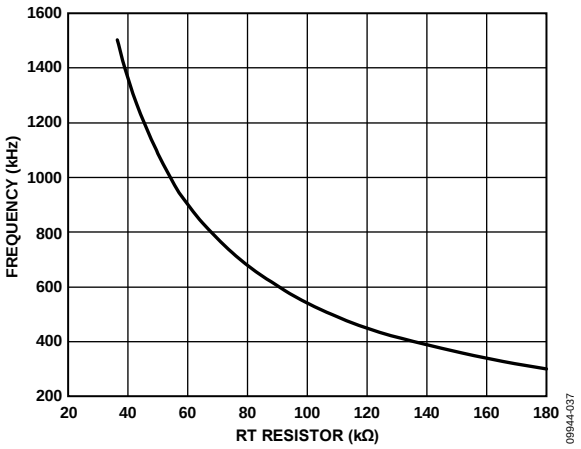


Figure 37. Switching Frequency vs. RT Resistor

To synchronize the ADP2164, drive an external clock at the SYNC pin. The frequency of the external clock can be in the range of 500 kHz to 1.4 MHz.

When the SYNC pin is driven by an external clock, the user can configure the switching frequency to be in phase with the external clock or 180° out of phase with the external clock, as follows:

- If the RT pin is connected to GND or to a resistor, the switching frequency is in phase with the external clock.
- If the RT pin is connected to VIN, the switching frequency is 180° out of phase with the external clock.

POWER GOOD

PGOOD is an active high, open-drain output and requires a resistor to pull it up to the logic supply voltage. PGOOD high indicates that the voltage on the FB pin (and, therefore, the output voltage) is within 10% of the desired value. PGOOD low indicates the opposite. There is a 16-cycle waiting period after the FB voltage is detected as being out of bounds. If FB returns to within the ±10% range, it is ignored by the PGOOD circuitry.

CURRENT LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2164 has a peak current limit protection circuit to prevent current runaway. The peak current limit is 6.2 A. When the inductor current reaches the peak current limit, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle begins.

The overcurrent counter is incremented by 1 at each peak current limit event. If the overcurrent counter exceeds 10, the part enters hiccup mode, and the high-side FET and low-side FET are both turned off. The part remains in this mode for 4096 clock cycles and then attempts to restart using soft start. If the current limit fault has cleared, the part resumes normal operation. If the current limit fault has not cleared, the part reenters hiccup mode after first counting 10 current limit violations.

OVERVOLTAGE PROTECTION (OVP)

Overvoltage protection (OVP) circuitry is integrated in the ADP2164. The output voltage is continuously monitored by a comparator through the FB pin, which is at 0.6 V (typical) under normal operation. The comparator is activated when the FB voltage exceeds 0.66 V (typical), thus indicating an output overvoltage condition. If the voltage remains above the OVP threshold for 16 clock cycles, the high-side MOSFET turns off and the low-side MOSFET turns on until the current through it reaches the −1.3 A current limit. Both MOSFETs remain in the off state until FB falls below 0.54 V (typical), after which the part restarts. The behavior of PGOOD under this condition is described in the Power Good section.

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage lockout (UVLO) circuitry is integrated in the ADP2164. If the input voltage falls below 2.5 V, the ADP2164 shuts down, and both the power switch and the synchronous rectifier turn off. When the voltage rises above 2.6 V again, the soft start is initiated, and the part is enabled.

THERMAL SHUTDOWN

If the ADP2164 junction temperature rises above 140°C, the thermal shutdown circuit turns off the regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, and/or high ambient temperature. When thermal shutdown occurs, a 15°C hysteresis ensures that the ADP2164 does not return to operation until the on-chip temperature falls below 125°C. Soft start is initiated when the part comes out of thermal shutdown.

APPLICATIONS INFORMATION

ADISIMPOWER DESIGN TOOL

The ADP2164 is supported by ADIsimPower design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can also request an unpopulated board through the tool.

The typical application circuit for the ADP2164 is shown in Figure 38.

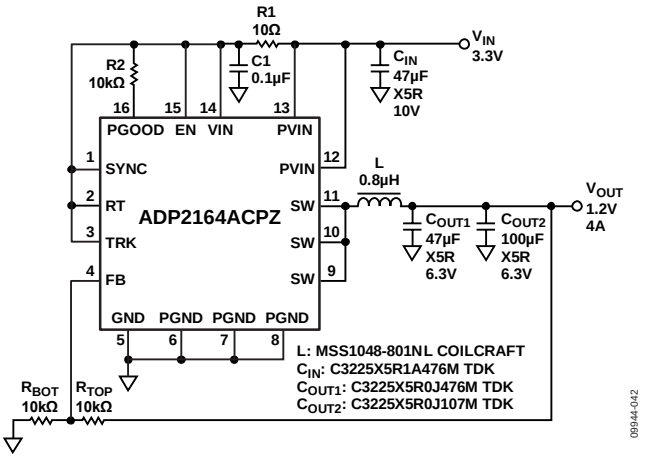


Figure 38. Typical Application Circuit

OUTPUT VOLTAGE SELECTION

The output voltage of the adjustable version of the ADP2164 is set by an external resistive voltage divider using the following equation:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

To limit output voltage accuracy degradation due to FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that R_{BOT} is less than 30 kΩ.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and ripple current. A small inductor value provides larger inductor current ripple and fast transient response but degrades efficiency; a large inductor value provides small inductor current ripple and good efficiency but slows transient response. For a reasonable trade-off between transient response and efficiency, the inductor current ripple, ΔI_L, is typically set to one-third the maximum load current. The inductor value is calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_S}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
ΔI_L is the inductor current ripple.
f_S is the switching frequency.
D is the duty cycle (V_{OUT}/V_{IN}).

The ADP2164 uses slope compensation in the current control loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

The negative current limit (−1.3 A) also limits the minimum inductor value. The inductor current ripple (ΔI_L) calculated by the selected inductor should not exceed 2.6 A.

The peak inductor current should be kept below the peak current limit threshold and is calculated using the following equation:

$$I_{PEAK} = I_O + \frac{\Delta I_L}{2}$$

Ensure that the rms current of the selected inductor is greater than the maximum load current and that its saturation current is greater than the peak current limit of the converter.

OUTPUT CAPACITOR SELECTION

The output capacitor value is determined by the output voltage ripple, load step transient, and loop stability. The output ripple is determined by the ESR and the capacitance.

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_S}\right)$$

The load step transient response depends on the inductor, the output capacitor, and the current control loop.

The ADP2164 has integrated loop compensation for simple power design. Table 5 and Table 6 show the recommended values for inductors and capacitors for the ADP2164 based on the input and output voltages for the part. X5R or X7R dielectric ceramic capacitors are highly recommended.

Table 5. Recommended L and C_{OUT} Values at f_S = 1.2 MHz

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)
3.3	1.0	0.8	100 + 100
3.3	1.2	0.8	100 + 47
3.3	1.5	1	100 + 47
3.3	1.8	1	100
3.3	2.5	1	47
5	1.0	0.8	100 + 100
5	1.2	0.8	100 + 47
5	1.5	1	100 + 47
5	1.8	1	100
5	2.5	1	47
5	3.3	1	47

Table 6. Recommended L and C_{OUT} Values at f_S = 600 kHz

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)
3.3	1.0	1	100 + 100
3.3	1.2	1	100 + 100
3.3	1.5	1	100 + 47
3.3	1.8	1	100 + 47
3.3	2.5	1	100
5	1.0	1	100 + 100
5	1.2	1.5	100 + 100
5	1.5	1.5	100 + 47
5	1.8	1.5	100 + 47
5	2.5	1.5	100
5	3.3	1.5	100

Higher or lower values of inductors and output capacitors can be used in the regulator, but system stability and load transient performance must be verified.

Table 7 and Table 8 list some recommended inductors and capacitors for the ADP2164.

Table 7. Recommended Inductors

Manufacturer	Part No.
Coilcraft®	MSS1038, MSS1048, MSS1260
Sumida	CDRH103R, CDRH104R, CDRH105R

Table 8. Recommended Capacitors

Manufacturer	Part No.	Description
Murata	GRM32ER60J107ME20	100 µF, 6.3 V, X5R, 1210
Murata	GRM32ER60J476ME20	47 µF, 6.3 V, X5R, 1210
TDK	C3225X5R0J107M	100 µF, 6.3 V, X5R, 1210
TDK	C3225X5R0J476M	47 µF, 6.3 V, X5R, 1210

INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on PVIN. Place the input capacitor as close as possible to the PVIN pins. A 22 µF or 47 µF ceramic capacitor is recommended. The rms current rating of the input capacitor should be larger than the value calculated using the following equation:

$$I_{RMS} = I_O \times \sqrt{D \times (1-D)}$$

where D is the duty cycle.

VOLTAGE TRACKING

The ADP2164 includes a tracking feature that allows the ADP2164 output (slave voltage) to be configured to track an external voltage (master voltage), as shown in Figure 39.

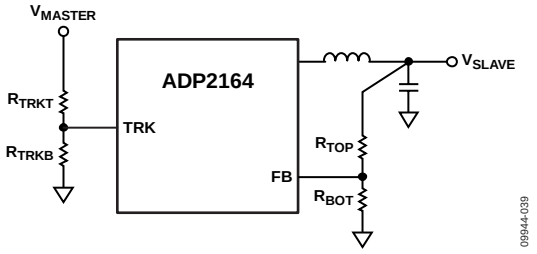


Figure 39. Voltage Tracking

Coincident Tracking

A common requirement is coincident tracking, as shown in Figure 40. Coincident tracking limits the slave output voltage to the same value as the master voltage until the slave output voltage reaches regulation. Connect the TRK pin to a resistor divider driven from the master voltage, as shown in Figure 39. For coincident tracking, set $R_{TRKT} = R_{TOP}$ and $R_{TRKB} = R_{BOT}$.

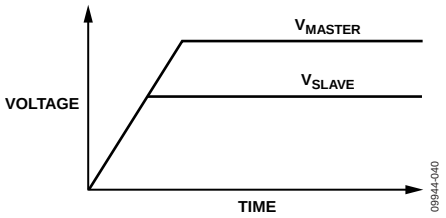


Figure 40. Coincident Tracking

Ratiometric Tracking

Ratiometric tracking is shown in Figure 41. The slave output is limited to a fraction of the master voltage. In this application, the slave and master voltages reach their final values at the same time.

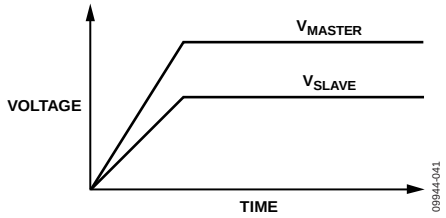


Figure 41. Ratiometric Tracking

The ratio of the slave output voltage to the master voltage is a function of the two dividers.

$$\frac{V_{SLAVE}}{V_{MASTER}} = \frac{1 + \frac{R_{TOP}}{R_{BOT}}}{1 + \frac{R_{TRKT}}{R_{TRKB}}}$$

APPLICATIONS CIRCUITS

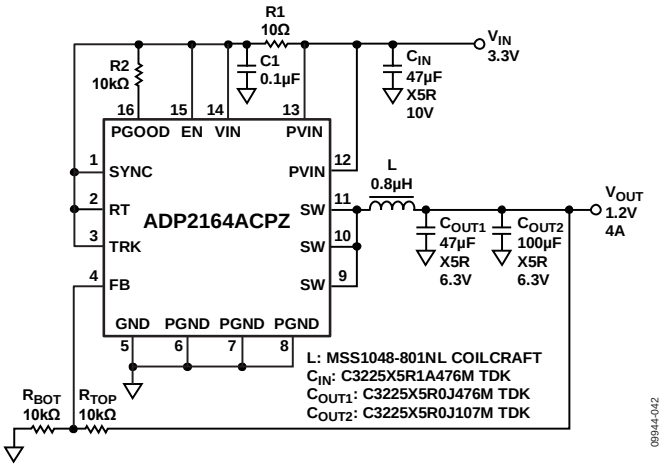


Figure 42. 1.2 V, 4 A, 1.2 MHz Step-Down Regulator

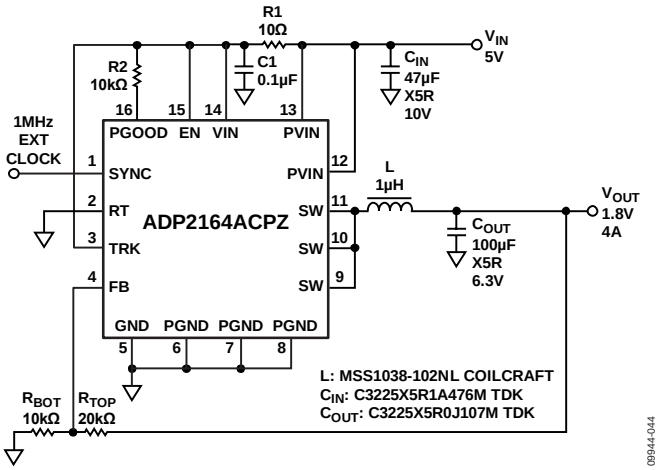


Figure 43. 1.8 V, 4 A Step-Down Regulator, Synchronized to 1 MHz, in Phase with the External Clock

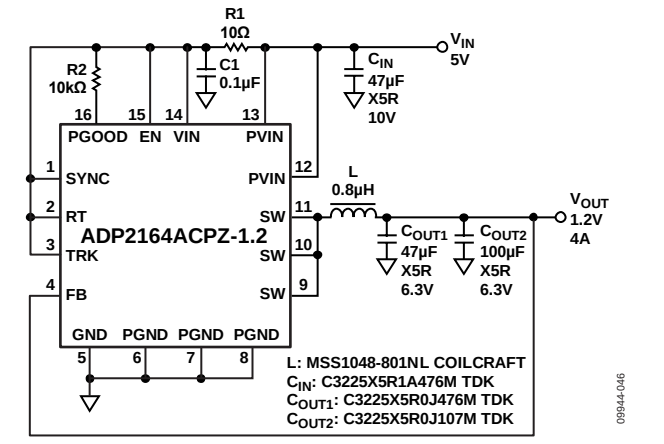


Figure 44. Fixed 1.2 V, 4 A, 1.2 MHz Step-Down Regulator

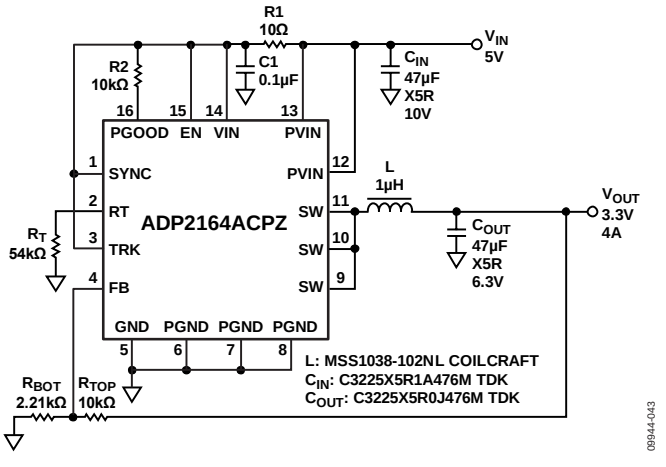


Figure 45. 3.3 V, 4 A, 1 MHz Step-Down Regulator

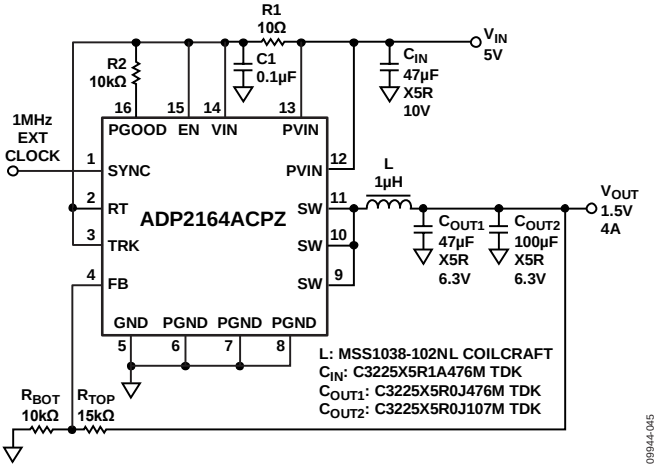


Figure 46. 1.5 V, 4 A Step-Down Regulator, Synchronized to 1 MHz, 180° out of Phase with the External Clock

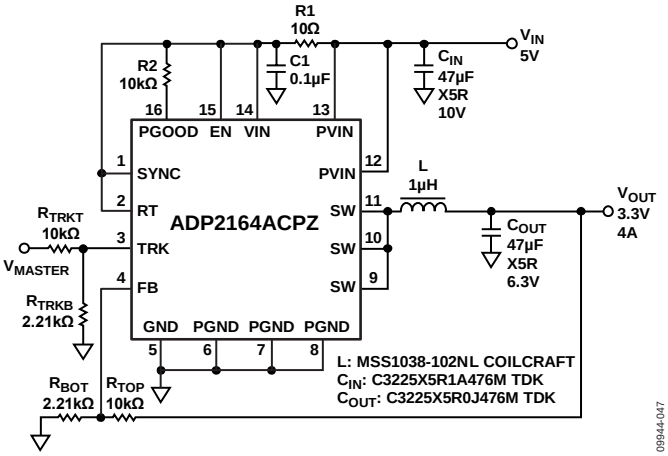
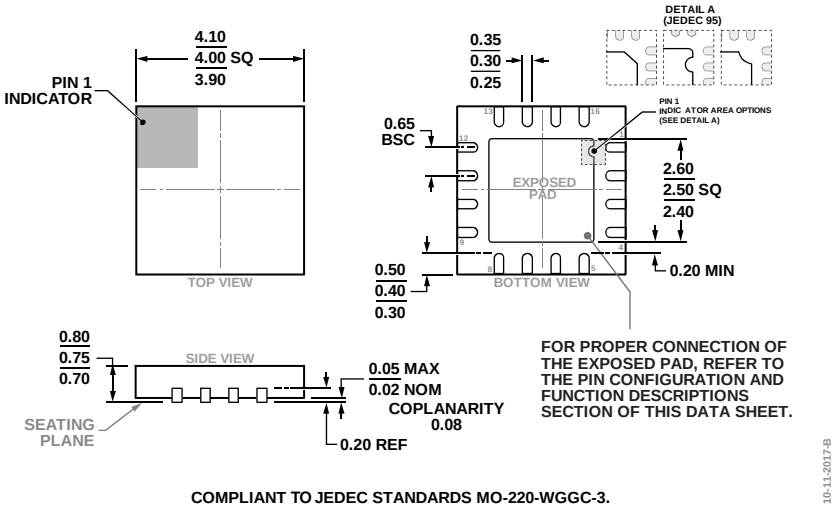


Figure 47. 3.3 V, 4 A, 1.2 MHz Step-Down Regulator, Tracking Mode

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC-3.

Figure 48. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage	Package Description	Package Option
ADP2164ACPZ-R7	−40°C to +125°C	Adjustable	16-Lead LFCSP	CP-16-26
ADP2164ACPZ-1.0-R7	−40°C to +125°C	1.0 V	16-Lead LFCSP	CP-16-26
ADP2164ACPZ-1.2-R7	−40°C to +125°C	1.2 V	16-Lead LFCSP	CP-16-26
ADP2164ACPZ-1.5-R7	−40°C to +125°C	1.5 V	16-Lead LFCSP	CP-16-26
ADP2164ACPZ-1.8-R7	−40°C to +125°C	1.8 V	16-Lead LFCSP	CP-16-26
ADP2164ACPZ-2.5-R7	−40°C to +125°C	2.5 V	16-Lead LFCSP	CP-16-26
ADP2164ACPZ-3.3-R7	−40°C to +125°C	3.3 V	16-Lead LFCSP	CP-16-26
ADP2164-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.

D09944-0-6/18(C)