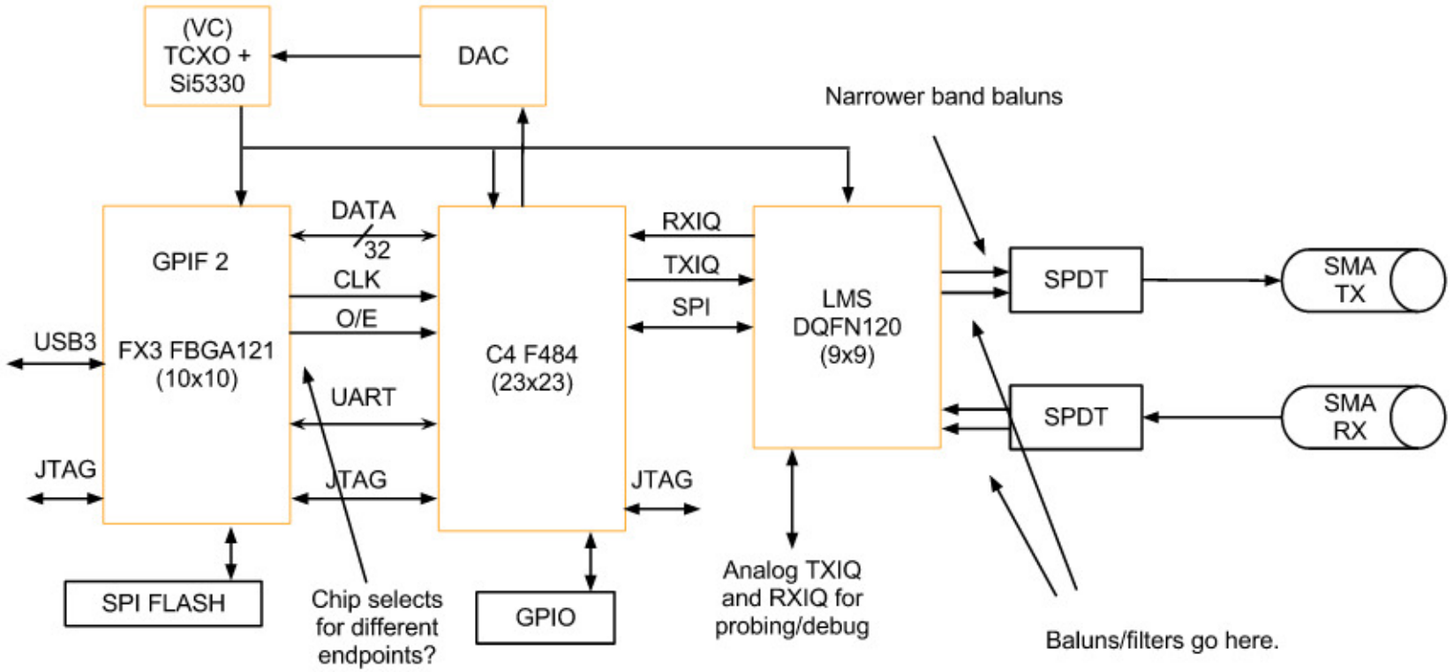
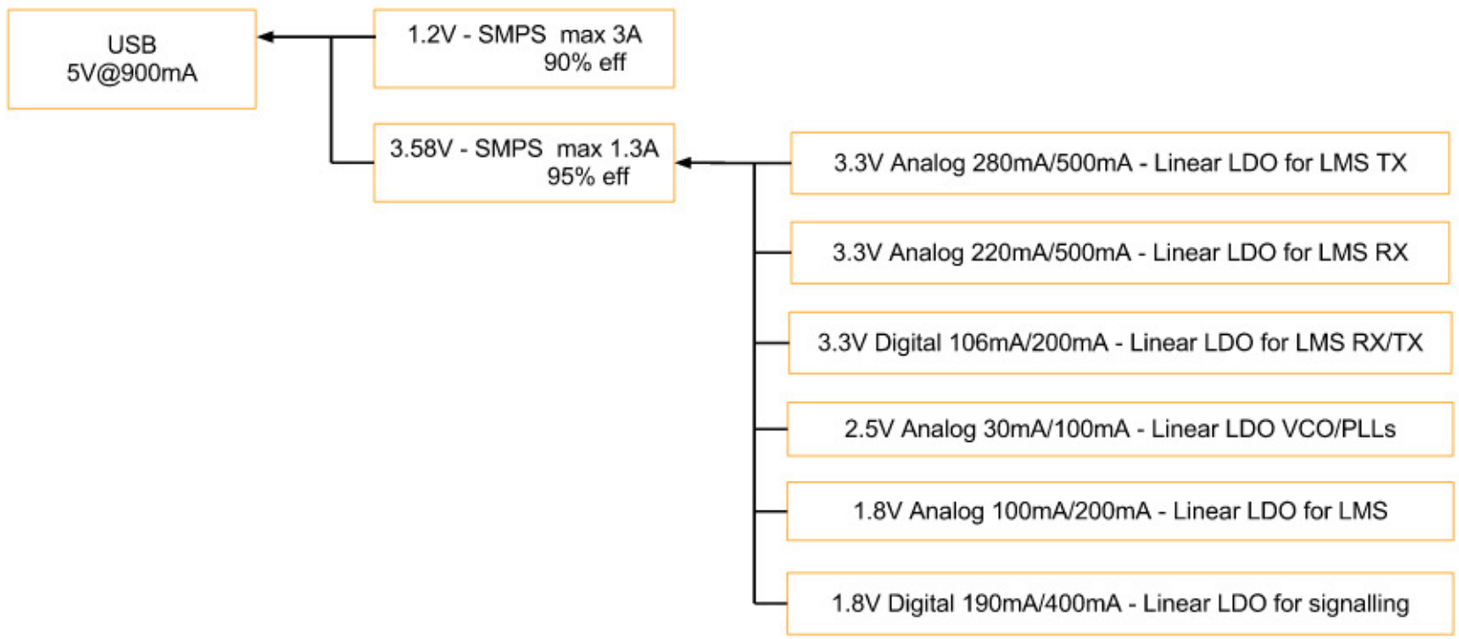
bladeRF - USB 3.0 Software Defined Radio





nuand

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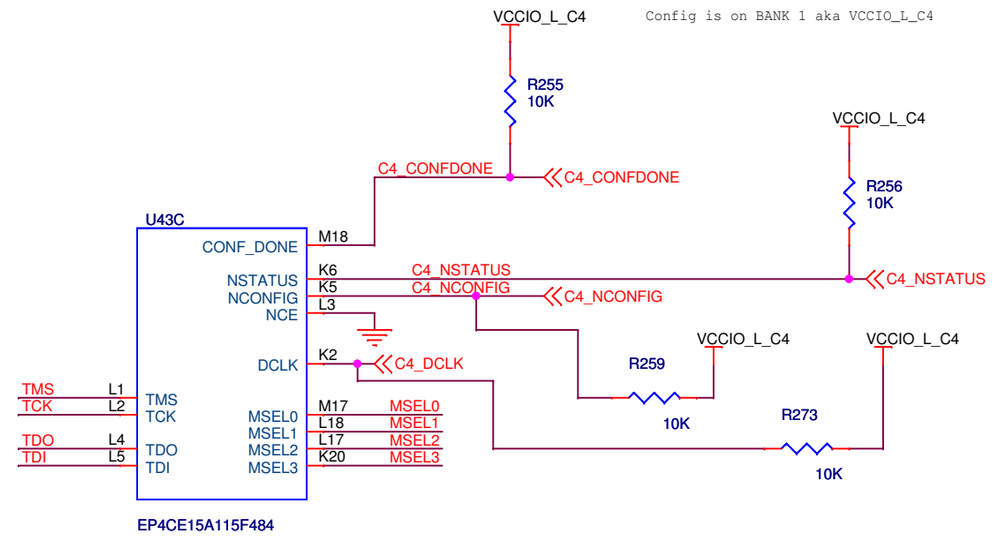
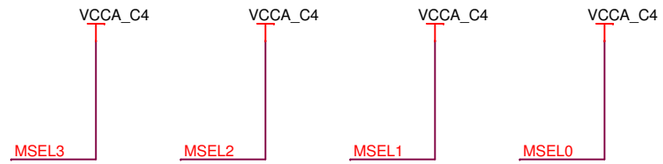
FPGA CONFIGURATION

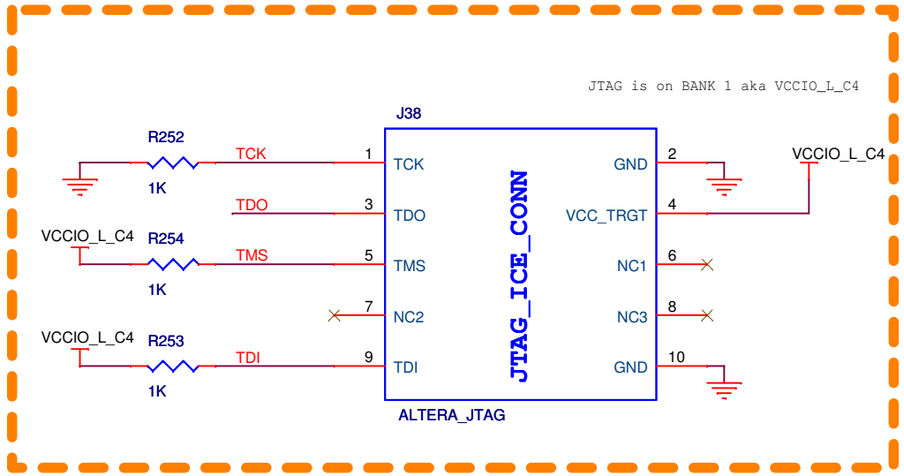


MSEL[3..0]



C4 handbook pg 171:
MSEL[3..0] =
PS-FAST = "1100" @ 3.3/3.0/2.5V
PS-STD = "0000" @3.3/3.0/2.5V
FPP-FAST = "1110" @3.3/3.0/2.5V
FPP-FAST = "1111" @1.8/1.5 V (default)

MSEL pins should be connected directly to VCCA or GND.



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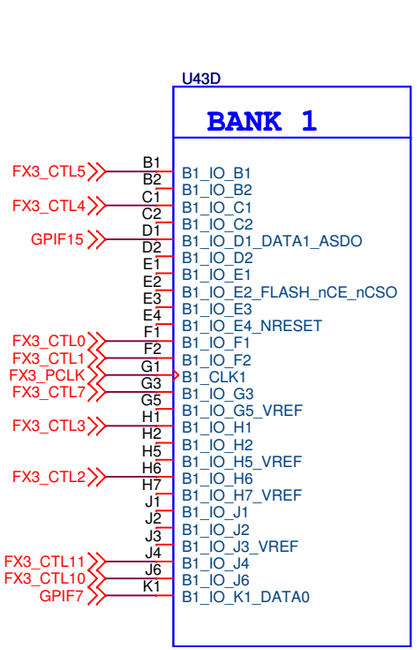
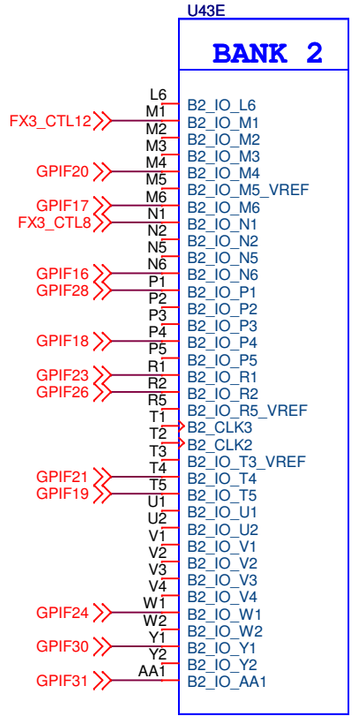
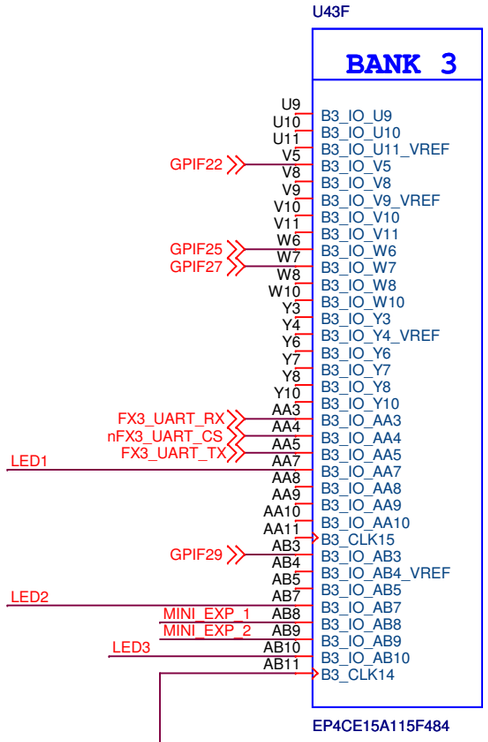
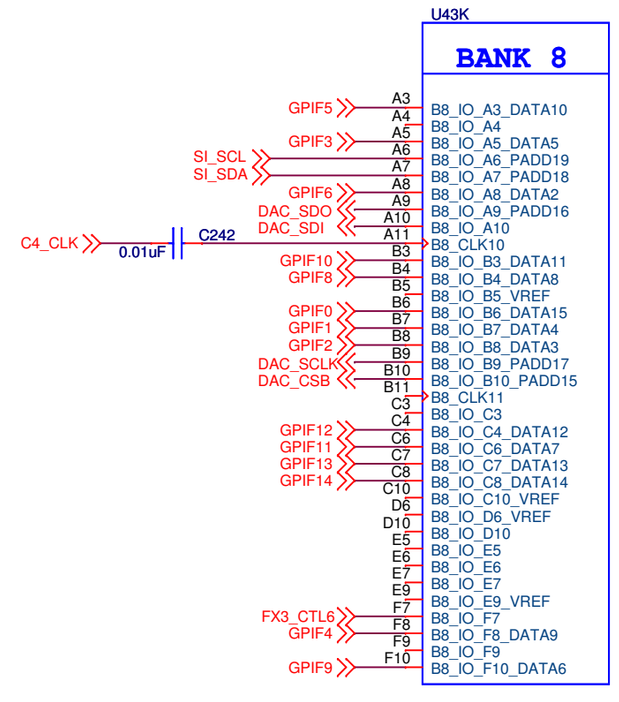
Avoid VREF pins due to their slow IO times.
UDCLK has to be a CTL pin.
DATA[0..7] have to be from GPIF[0..15]

FPGA "LEFT" BANK

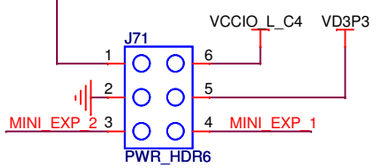


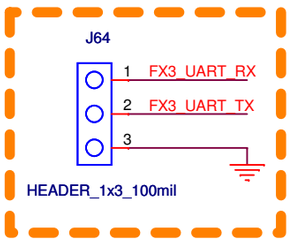


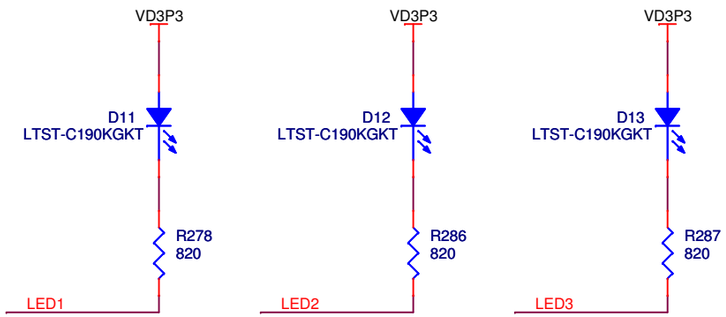




Mini Expansion Header







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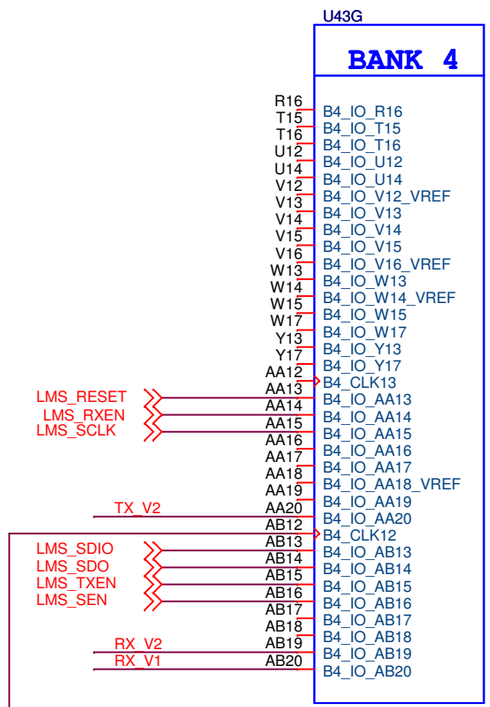
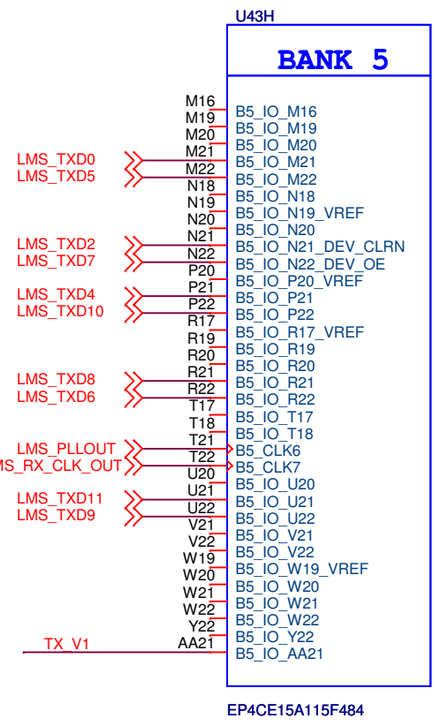
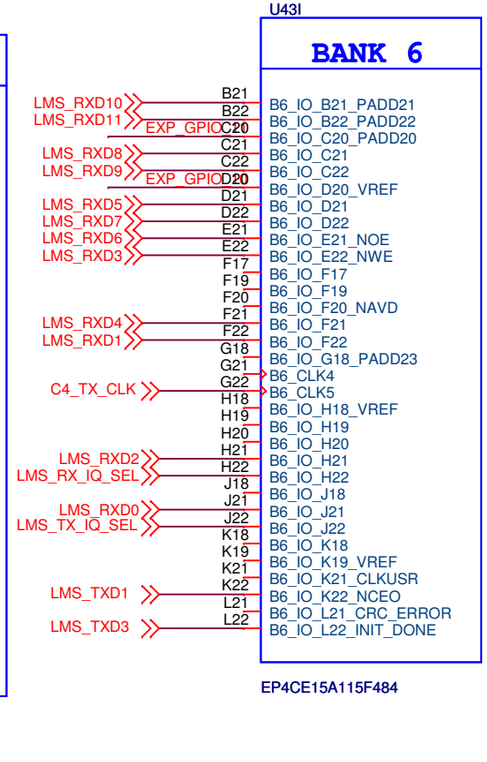
FPGA "RIGHT" BANK

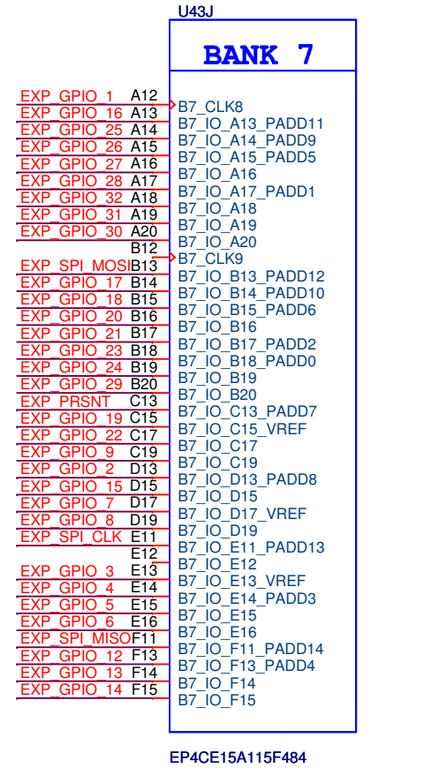
Avoid VREF pins due to their slow IO times.

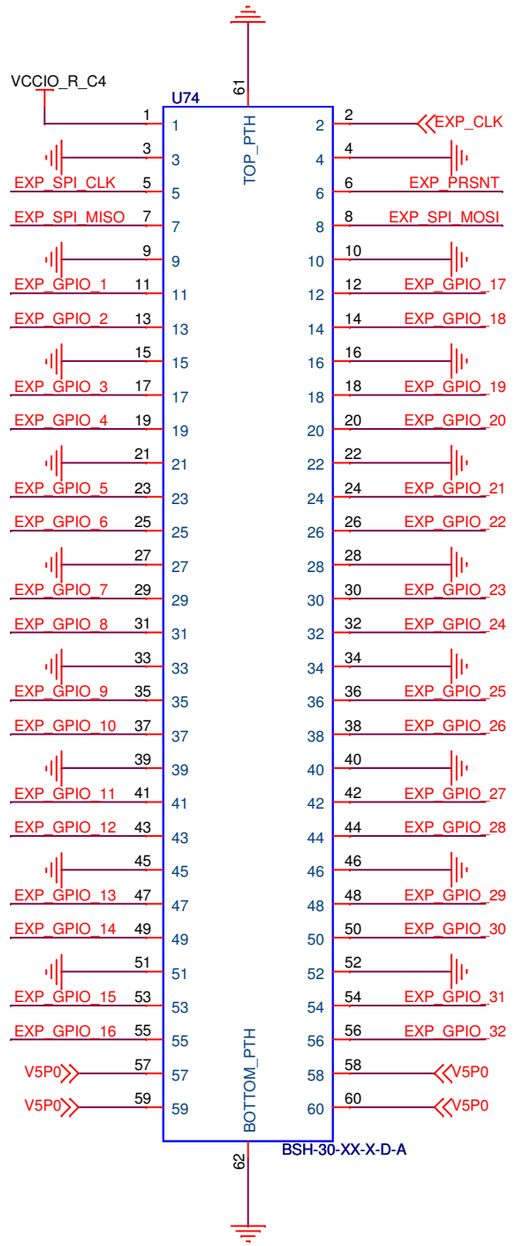
LMS SIGNALS GO TO THE "RIGHT" OF THE C4
BANKS 4, 5, 6, 7

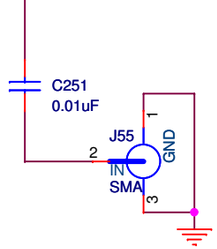


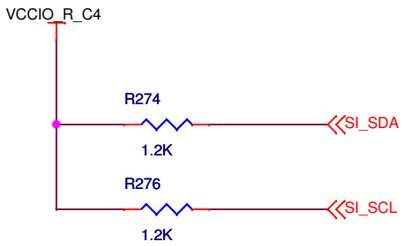


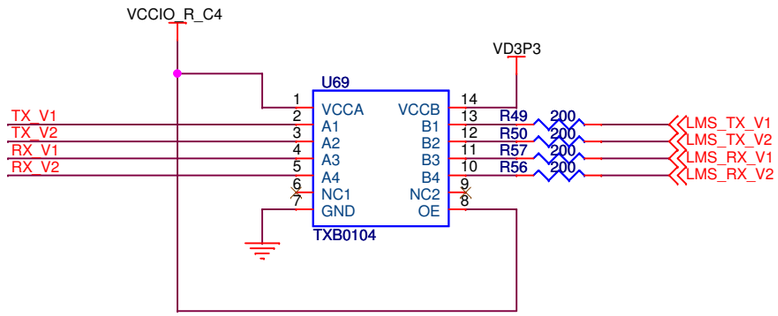












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FPGA POWER

VCCIO_L_C4 defines the "left" banks of the C4
VCCIO_R_C4 defines the "right" banks of the C4
The left side goes to the FX3, and the right side goes to the LMS.

VCCINT @1.2V, MAX 3.1A
VCCA2P5 @ 2.5, MAX 0.1A
VCCIO @1.8V MAX 0.1A

This power condition is for the 115KE part at 3A

Tantalum Tantalum Tantalum Tantalum

4V Tantalum 4V Tantalum

EP4CE15A115F484 EP4CE15A115F484

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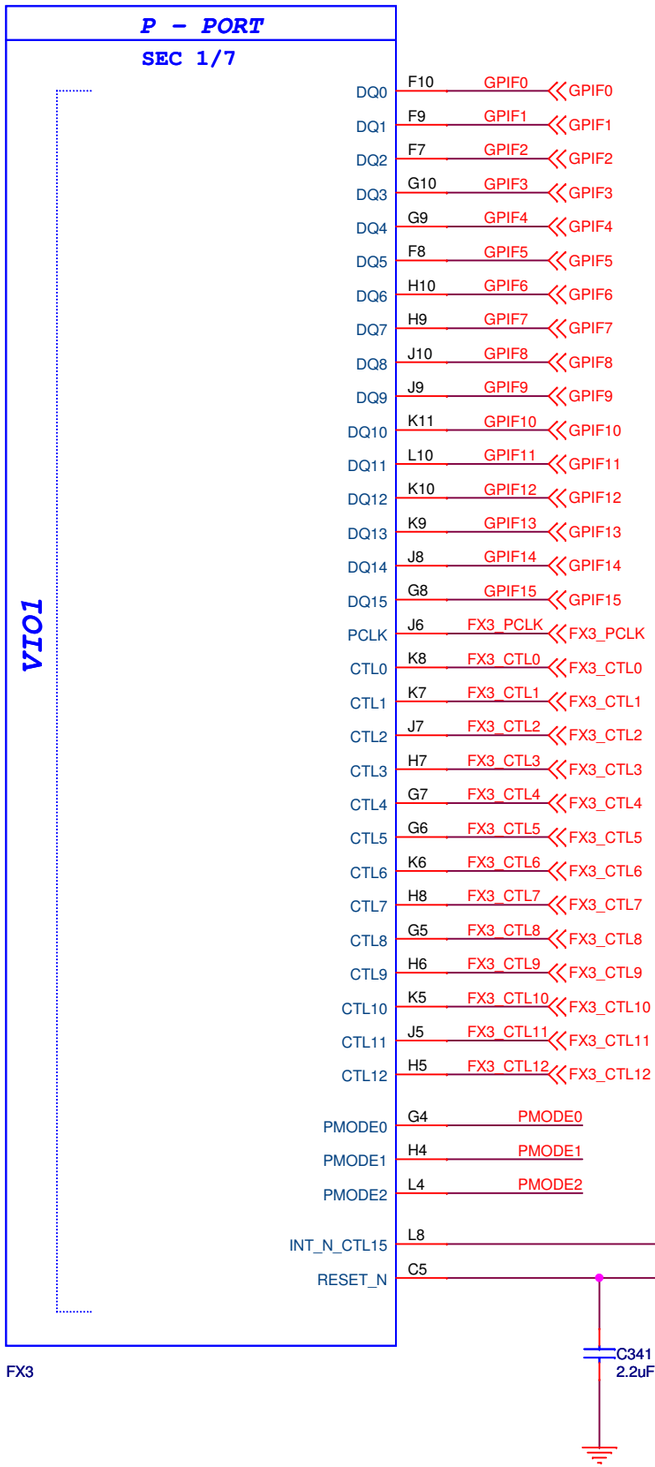
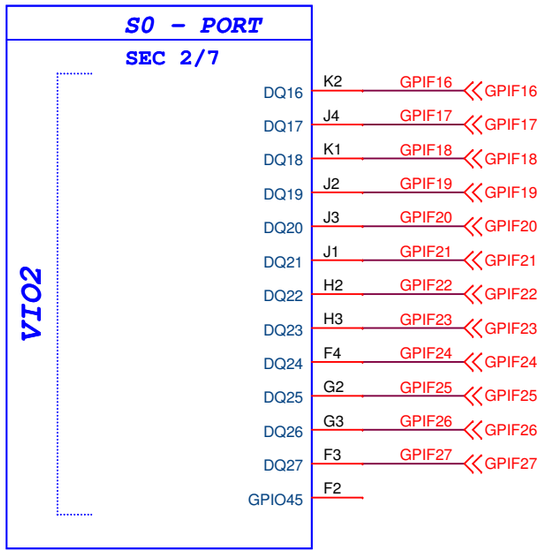
FX3 GPIF + BOOT

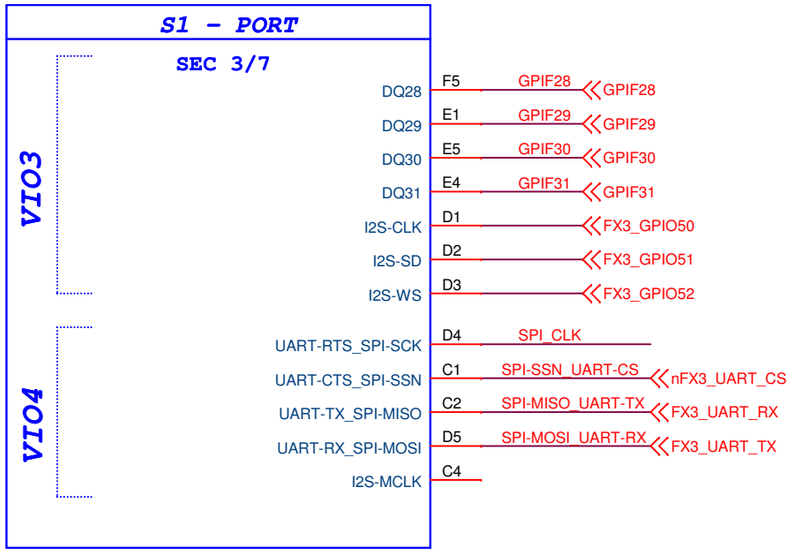
U2A



U2B

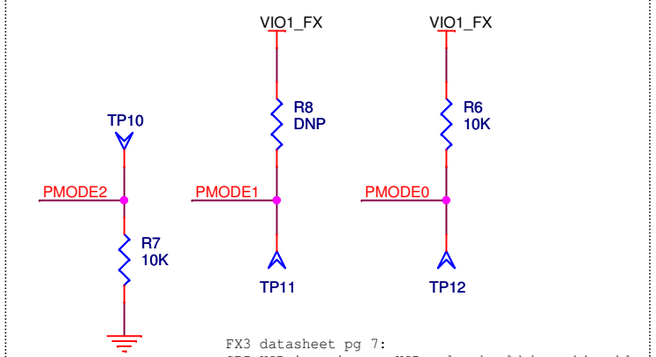


U2C



In 32-bit GPIF mode UART is (FX3 data pg 33):
GPIO[55](C2)=UART_TX
GPIO[56](D5)=UART_RX
UART_CS was added to allow the FPGA to use the
MISO/MOSI lines to communicate via UART with the FX3.
CS can also be deasserted to write to flash after boot.

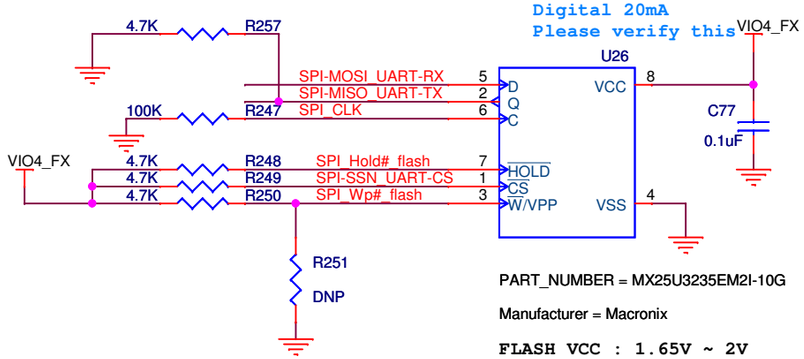
PMODE[2..0]



FX3 datasheet pg 7:
SPI+USB is primary, USB only should be achievable
SPI+USB on failure - PMODE[2:0] = "0F1"
USB boot - PMODE[2:0] = "F11"

Add R257 so that SPI-boot works. C4's HIGH-Z state has a
weak pull up, so it can be balanced out with a weak pull-down.

SPI Flash



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FX3 DEBUG + CLOCK SEL

U2F

MISC

SEC 6/7

VIO5

I2C-GPIO58_SCL	D9	FX3_I2C_SCL
I2C-GPIO59_SDA	D10	FX3_I2C_SDA
I2C-GPIO60_CHARGER-DETECT	D11	CHARGER_DETECT
TCK	F6	TCK
TDI	E7	TDI
TDO	C10	TDO
TMS	E8	TMS
TRST_N	B11	TRST_N

FX3

DEBUG TPs

CHARGER_DETECT — TP6

Debug LED

FX3_I2C_SCL — D10 LTST-C190KGKT

FSLC[2..0]

CVDDQ — R1 10K — FSLC2

CVDDQ — R2 10K — FSLC1

FSLC0 — R3 10K

FX3 datasheet pg 8:
38.4MHz input CLK - FSLC[2:0] = "110"

FX3 JTAG

VIO5_FX — R51 10K, R52 10K, R53 10K, R54 10K, R55 10K

J51 JTAG_ICE_CONN

1	VT_REF	V_SUPPLY	2
TRST_N 3	N_TRST	GND1	4
TDI 5	TDI	GND2	6
TMS 7	TMS	GND3	8
TCK 9	TCK	GND4	10
RTCK 11	RTCK	GND5	12
TDO 13	TDO	GND6	14
N_SRST 15	N_SRST	GND7	16
17	DBGRQ	GND8	18
19	DBGACK	GND9	20

N2520-6002-RB

PART_NUMBER = N2520-6002-RB
Manufacturer = 3M

FPGA Version Resistor

FX3_I2C_SDA — R310 DNP

U2E

XTAL / CLK

SEC 5/7

CVDDQ

FSLC0	B2	FSLC0
FSLC1	B4	FSLC1
FSLC2	E6	FSLC2
XTALIN	C6	XTALIN
XTALOUT	C7	XTALOUT
CLKIN	D7	C232 0.01uF FX3_CLK
CLKIN_32	D6	CLKIN_32

FX3

TP3 — FSLC2

TP2 — FSLC1

TP1 — FSLC0

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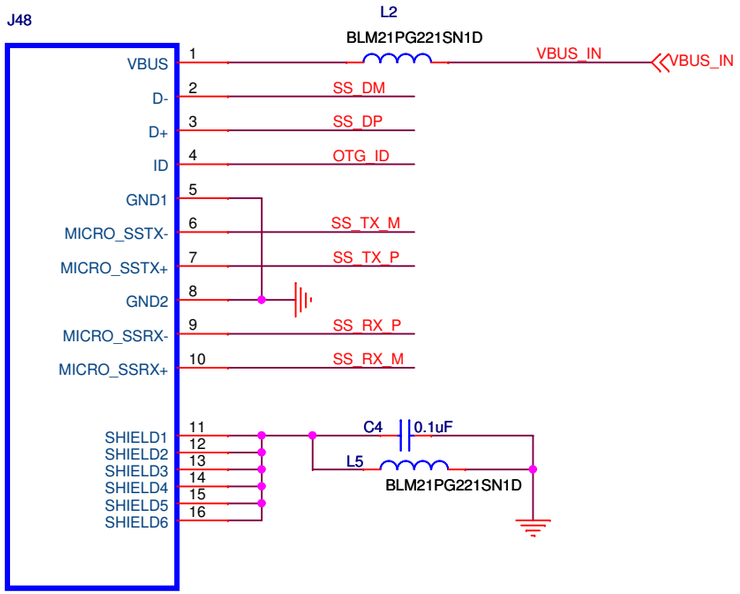
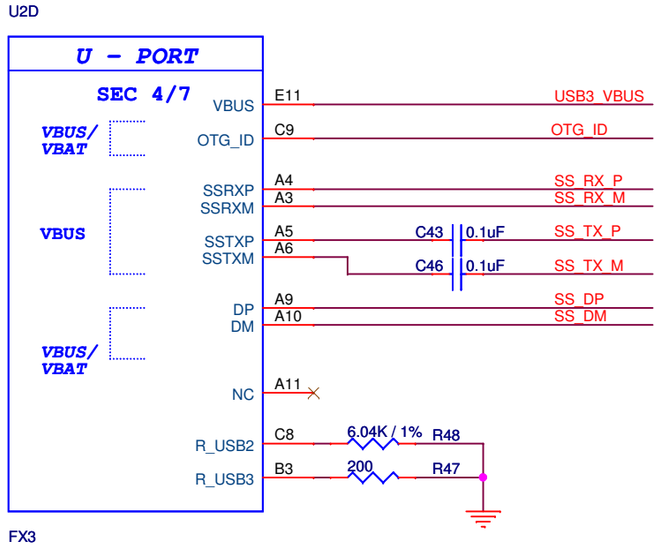
USB CONNECTIONS

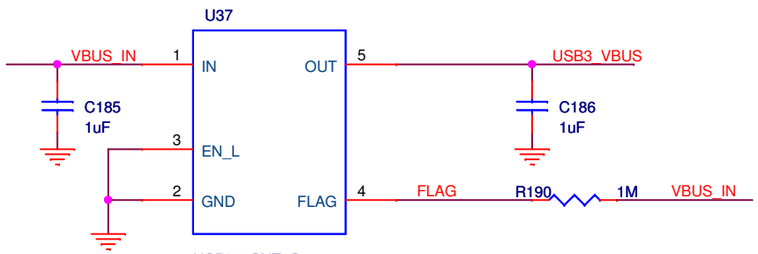
USB3.0 MICRO TYPE B



PART_NUMBER = GSB343133HR
Manufacturer = Amphenol
USB_3



USB Positive Overvoltage Protection Controller

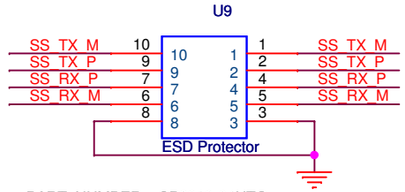


NCP361SNT1G

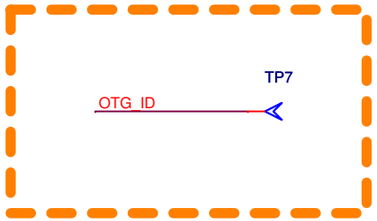
PART_NUMBER = NCP361SNT1G

Manufacturer = ON Semiconductor

ESD DEVICE



PART_NUMBER = SP3010-04UTG
Manufacturer = Littlefuse



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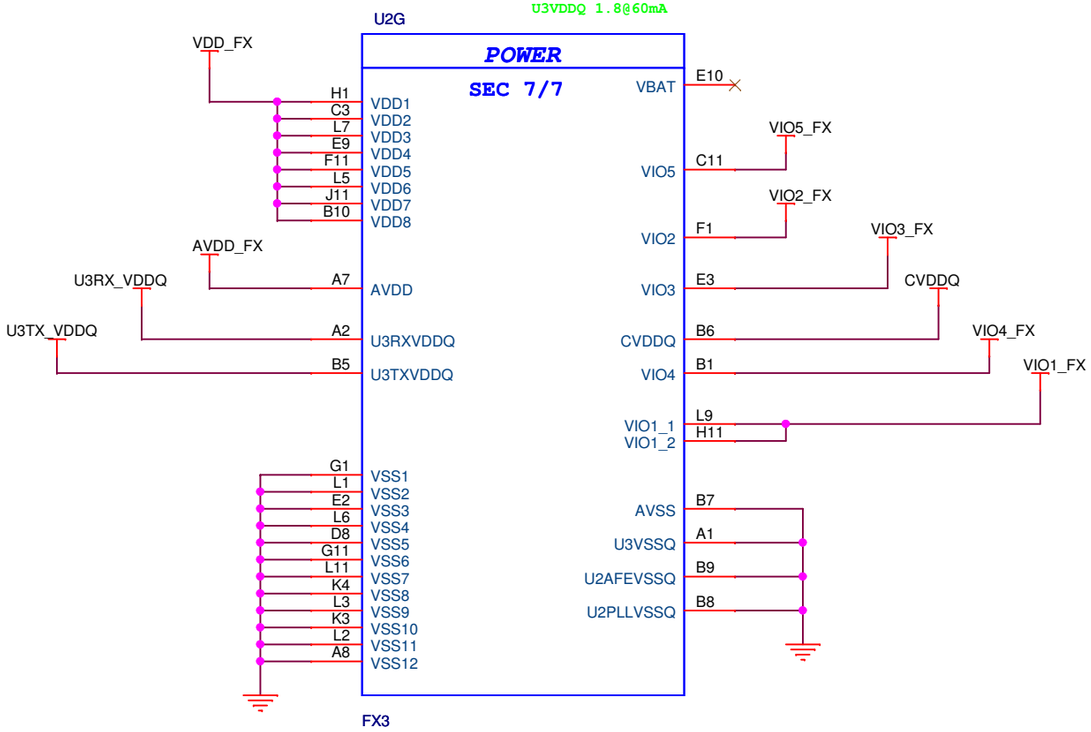
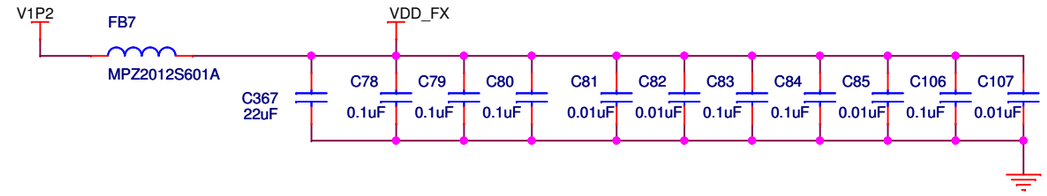
FX3 POWER

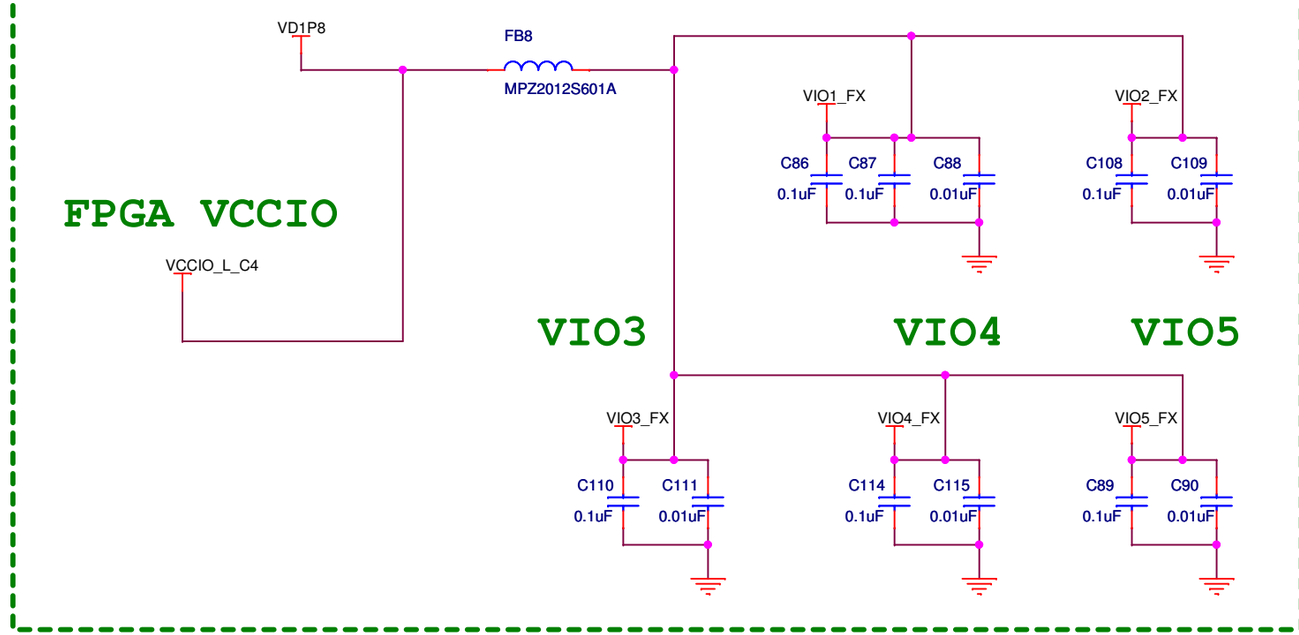
VDD+AVDD 1.2V@200mA
U3VDDQ 1.8@60mA



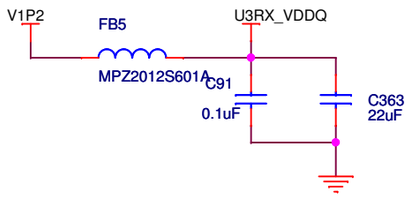
VDD



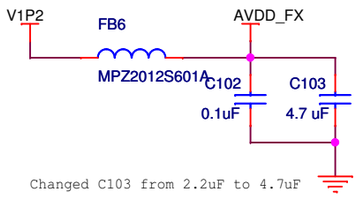
FPGA VCCIO



U3RX_VDDQ

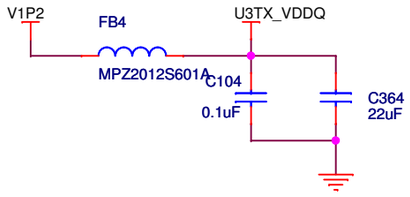


AVDD

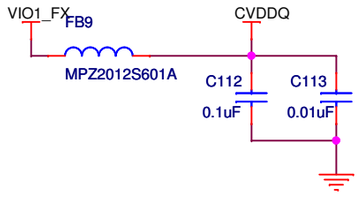


Changed C103 from 2.2uF to 4.7uF

U3TX_VDDQ



CVDDQ




```
U3RX_VDDQ  = V1P2
U3TX_VDDQ  = V1P2
AVDD       = V1P2
CVDDQ      = V1P8
VDD        = V1P2
VIO1       = V1P8
VIO2       = V1P8
VIO3       = V1P8
VIO4       = V1P8
VIO5       = V1P8
```

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LMS DIGITAL

Analog 1.8V
Analog 40mA

VA1P8
L20 MMZ0603S601C
R260
22
TXVDDVCO18
C205 10uF
C200 0.1uF
L21 MMZ0603S601C
R261
22
RXVDDVCO18
C206 10uF
C201 0.1uF

Digital 1.8V
Digital 45.51mA

VD1P8
L19 MMZ0603S601C
L16 MMZ0603S601C
RAVDD18
RXVCCPLL18
C199 1uF
C196 0.1uF
L18 MMZ0603S601C
L15 MMZ0603S601C
L17 MMZ0603S601C
C198 0.1uF
C195 0.1uF
C197 0.1uF

PLLCLK is Vref'd by PVDDSPI33

LMS_CLK
C231 0.01uF
71 PLLCLK

U1B

LMS_TXEN	LMS_TX_EN	66	TXEN
LMS_TX_CLK	LMS_TX_CLK	19	TX_CLK
LMS_TX_IQ_SEL	LMS_TX_IQ_SEL	20	TX_IQ_SEL
LMS_TXD0	LMS_TXD0	21	TXD0
LMS_TXD1	LMS_TXD1	22	TXD1
LMS_TXD2	LMS_TXD2	23	TXD2
LMS_TXD3	LMS_TXD3	24	TXD3
LMS_TXD4	LMS_TXD4	25	TXD4
LMS_TXD5	LMS_TXD5	26	TXD5
LMS_TXD6	LMS_TXD6	27	TXD6
LMS_TXD7	LMS_TXD7	28	TXD7
LMS_TXD8	LMS_TXD8	29	TXD8
LMS_TXD9	LMS_TXD9	30	TXD9
LMS_TXD10	LMS_TXD10	31	TXD10
LMS_TXD11	LMS_TXD11	32	TXD11

R290 DNP
LMS_RXEN
R289 DNP
LMS_RESET
LMS_RESET 75 RESET
R288 100K

LMS_SEN	LMS_SEN	67	SEN
LMS_SCLK	LMS_SCLK	70	SCLK
LMS_SDIO	LMS_SDIO	69	SDIO
LMS_SDO	LMS_SDO	68	SDO

RXEN	76	LMS_RXEN
RX_CLK	17	LMS_RX_CLK
RX_IQ_SEL	16	LMS_RX_IQ_SEL
RXD0	15	LMS_RXD0
RXD1	14	LMS_RXD1
RXD2	13	LMS_RXD2
RXD3	10	LMS_RXD3
RXD4	11	LMS_RXD4
RXD5	8	LMS_RXD5
RXD6	9	LMS_RXD6
RXD7	6	LMS_RXD7
RXD8	5	LMS_RXD8
RXD9	4	LMS_RXD9
RXD10	3	LMS_RXD10
RXD11	2	LMS_RXD11

RX_CLK_OUT 40 LMS_RX_CLK_OUT → LMS_RX_CLK_OUT

TSTD_OUT2 77 → TP13
TSTD_OUT1 65 → TP14

LMS6002D

Digital 1.8V
Total 22mA

Analog 3.3V
Analog 573.547mA

U1A

33	RDVDD18	TXVCCLPF33	43
61	TXVCCPLL18	TXVCCMIX33	45
72	TRXVDDDSM18	TXVCCDRV33	49
73	VSPI18	TXPVDD33	47
83	RXVCCPLL18		
35	RAVDD18	RXVCCMIX33	90
36	TDVDD18	RXVCCLNA33	101
		RXPVDD33	107
		RXVCCTIA33	109
		RXVCCLPF33	111
		RXVCCVGA33	112
60	TXVDDVCO18		
84	RXVDDVCO18		
		TXPVDDPLL33A	58
		TXPVDDPLL33B	62
		TXVCCVCO33	59
		TXVCCCHP33	63
37	TAVDD33		
74	PVDDSPI33		
		RXVCCCHP33	78
		RXVCCLOB33	79
		RXVCCVCO33	82
		RXVCCPLL33	85
		RXPVDDPLL33A	86
		RXPVDDPLL33B	81
7	PVDDVGG		
1	PVDDAD33A		
12	PVDDAD33B		
18	PVDDAD33C		
34	PVDDAD33D	GLOBAL_GND	117

LMS6002D

PVDDAD33[A-D] are the ADC/DAC IO buf Vref pins

V3P3_TX_LMS
L23 MMZ0603S601C
C203 1uF

PVDDVGG must be 3.3V

VD3P3
L57 MMZ1005S601C
C204 1uF

VCCIO_R_C4
L22 MMZ0603S601C
VCCIO_R_C4_CLK
L24 MMZ0603S601C
PVDDSPI33 is a Vref for the SPI + PLLCLK. Pin 71,74 need split plane
C202 0.1uF
C247 0.1uF

22mA

VD1P8
VCCIO_R_C4
L25 MMZ0603S601C
L26 MMZ0603S601C
Pin 34 is further away from the other pins so parts are replicated
C208 1uF
C207 1uF

V3P3_TX_LMS
L9 MMZ0603S601C
L10 MMZ0603S601C
C189 0.1uF
C190 0.1uF

V3P3_RX_LMS
L7 MMZ0603S601C
L8 MMZ0603S601C
C187 0.1uF
C188 0.1uF

ESD supply higher current
Needs MPZ2012S601A

V3P3_RX_LMS
L30 MMZ0603S601C
L56 MMZ1005S601C
L14 MMZ0603S601C
C192 0.1uF
C193 0.1uF
C194 0.1uF

V3P3_TX_LMS
L11 MMZ0603S601C
C191 0.1uF

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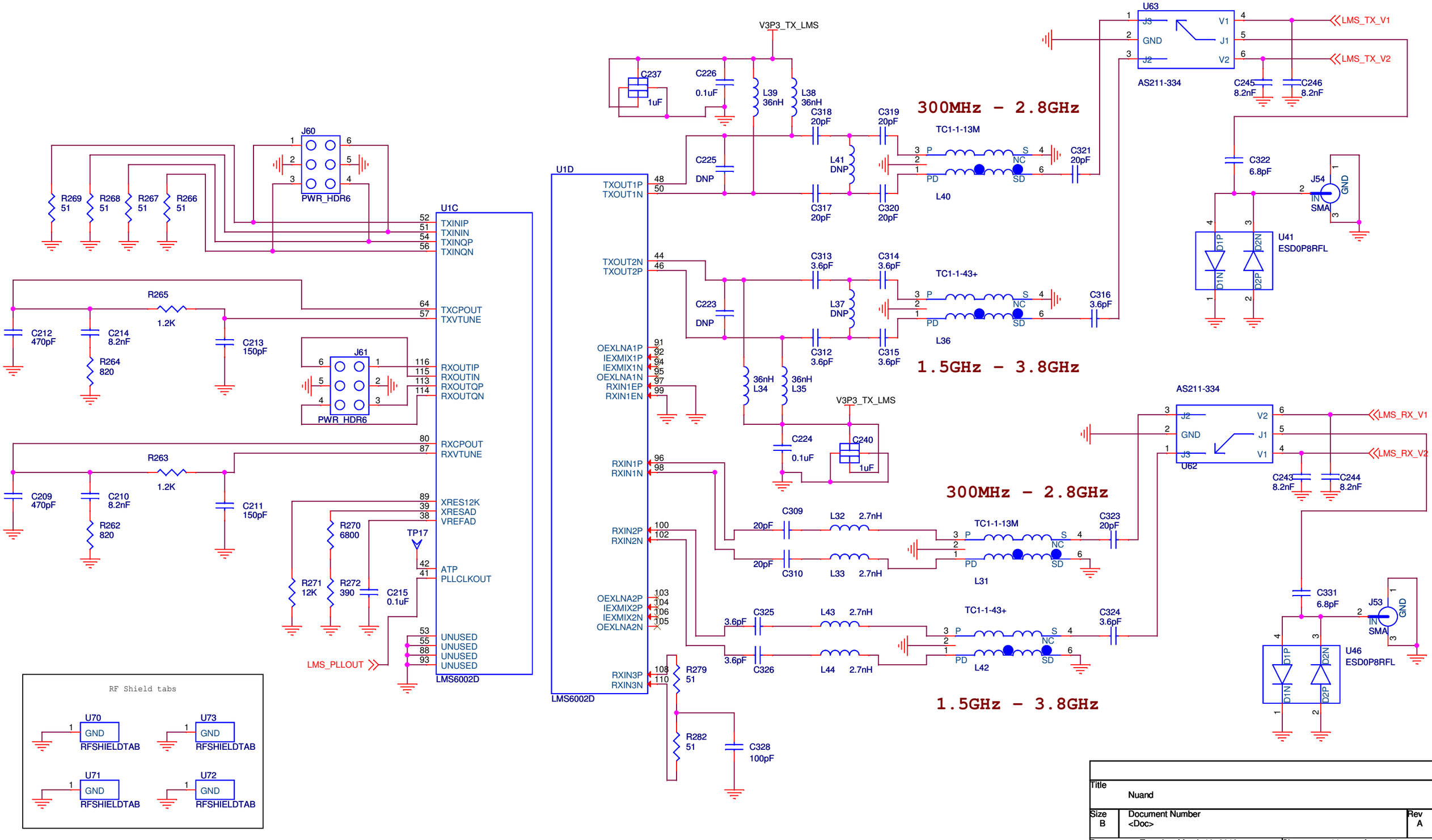
LMS ANALOG + RF



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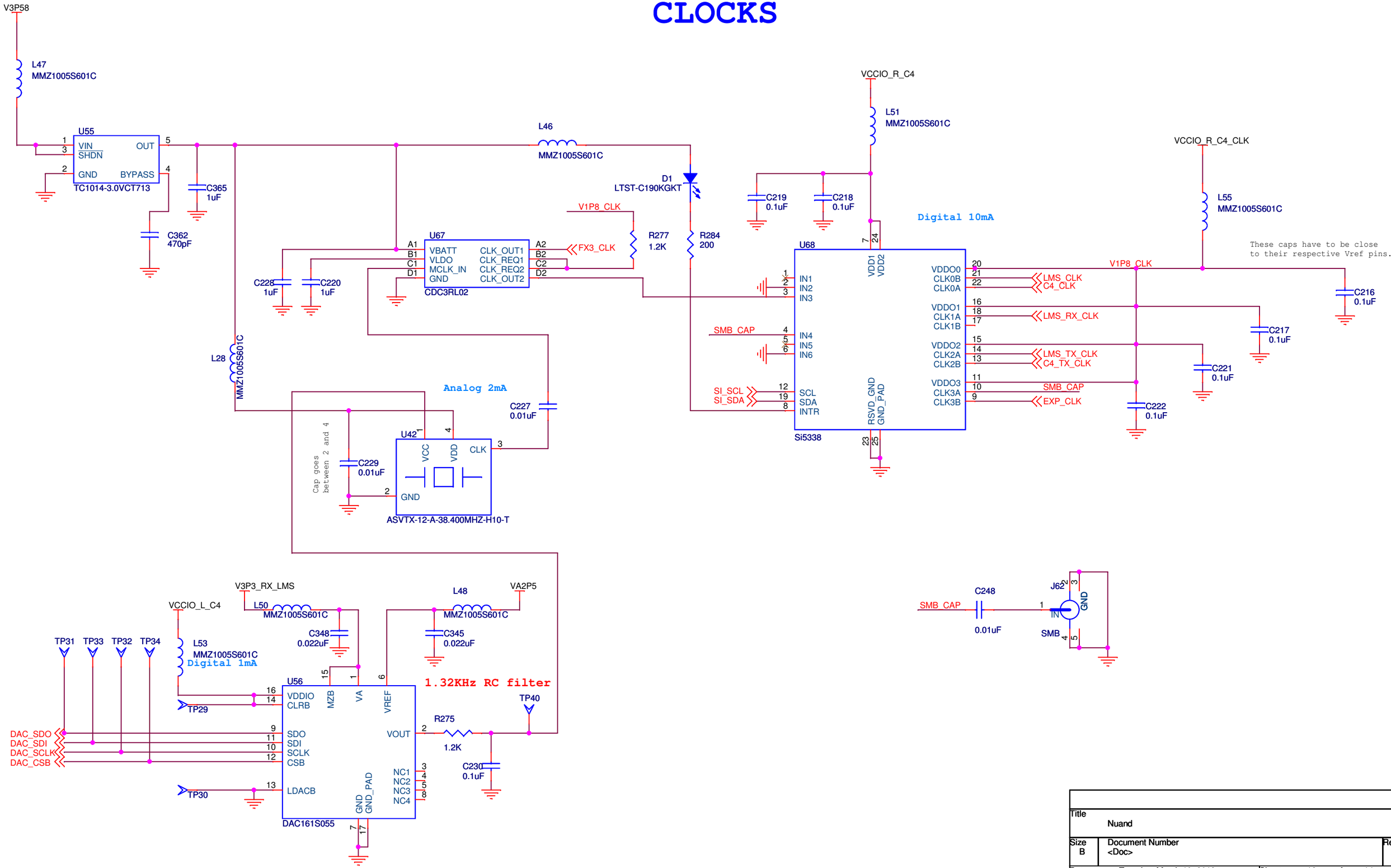
CLOCKS



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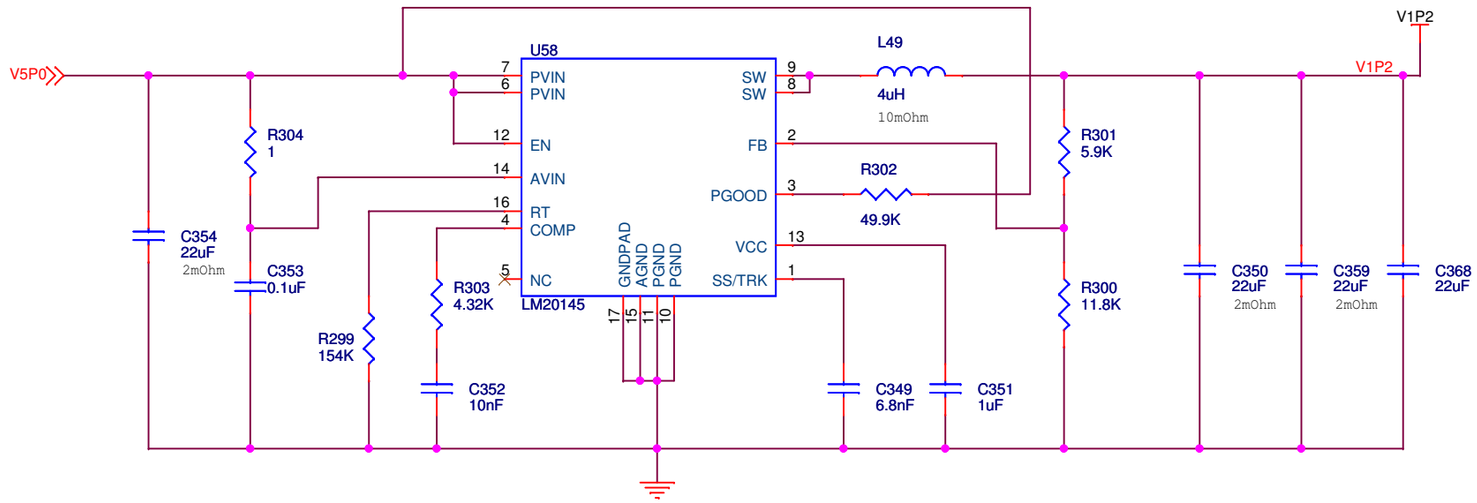
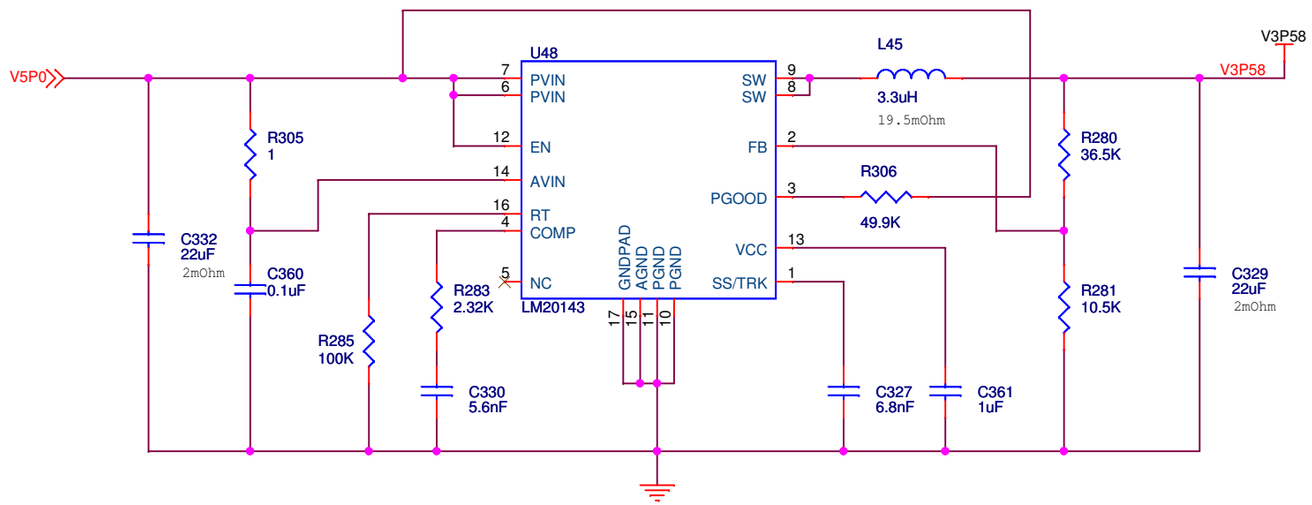
POWER DISTRIBUTION

The idea is to drop to 1.2V and 3.58V with SMPS.
Then drop to 3.3, 2.5, 1.8 from the 3.58V SMPS.

1.2V (min:200mA, typ:800mA) / 3100mA / 90% eff

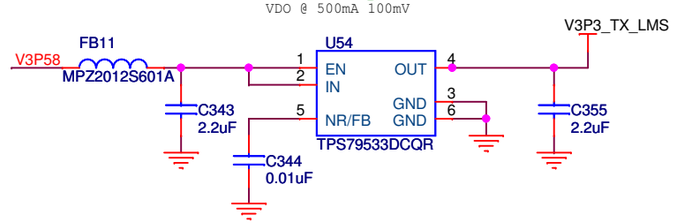


3.58V ~800mA / 1300mA / 95% eff



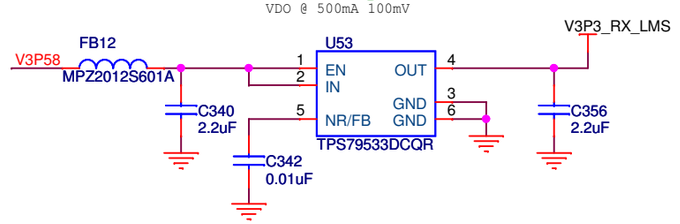
Analog 3.3V 280mA / 500mA

VDO @ 500mA 100mV



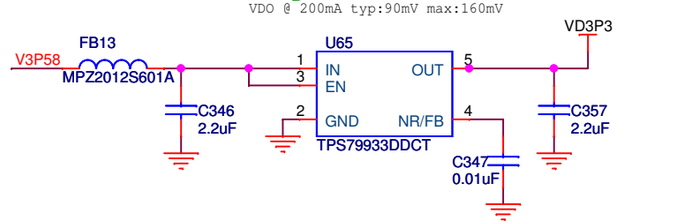
Analog 3.3V 220mA / 500mA

VDO @ 500mA 100mV



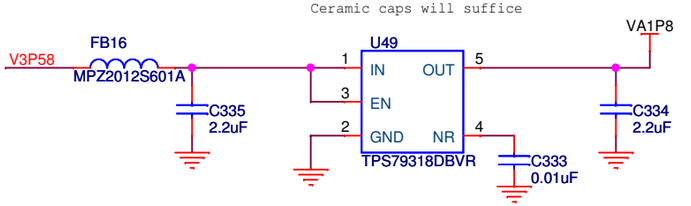
Digital 3.3V 106mA / 200mA

VDO @ 200mA typ:90mV max:160mV



Analog 1.8V ~100mA / 200mA

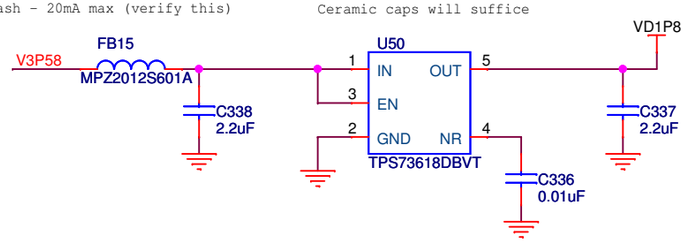
Ceramic caps will suffice



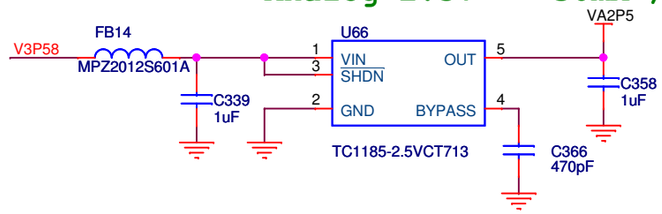
LMS - 67.1mA
FPGA - 25mA
FX3 - 25 mA
Clocks - XOs - 20mA
SPI flash - 20mA max (verify this)

Digital 1.8V 190mA / 400mA

Ceramic caps will suffice



Analog 2.5V 30mA / 100mA



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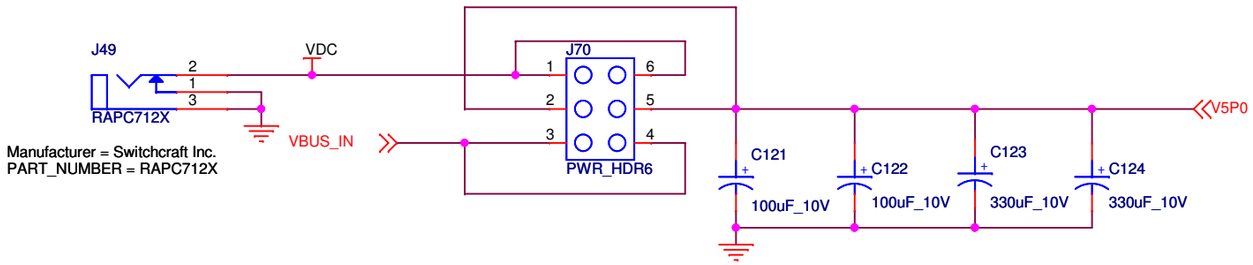
POWER SELECTION + DEBUG

Jumpered power selection
DC barrel vs USB3 bus



Scatter these testpoints throughout the design.
Testpoints will be PTH

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