Chapter 10. Radiation Effects in MMIC Devices

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I. Introduction

The use of microelectronic devices in both civilian and military spacecraft requires that these devices preserve their functionality in the hostile space environment throughout the mission life. An important feature of this environment is the presence of radiation of various types, including that from man-made sources. Unlike other aspects of reliability discussed in this chapter, radiation is unique and is not a requirement for nearly all other high-reliability applications, such as automotive, medical and terrestrial communications. Thus, because of the distinctive nature of the radiation environment, it is important to understand the effects of radiation on microelectronic devices and circuits, in particular on MMIC devices, used in space systems.

In this chapter we present a summary of the current understanding of the effects of radiation on MMIC devices. We begin with very brief background discussions of the radiation environment, and of the more "classical" microelectronic radiation effects found in Si-based devices, especially digital CMOS. As we pursue our discussion of radiation effects in MMIC devices, we will also briefly contrast these effects with those in other III–V-based technologies such as GaAs digital and III–V photonic devices.

II. Radiation Environments and Sources

Because this guideline is intended primarily for space applications, our focus in this discussion will be on the natural space-radiation environment. However, it is important to remember that there are other important sources of radiation. For example, many military space assets must be designed to maintain functionality in the presence of an environment that is enhanced by nuclear weapons. This enhanced environment has been discussed in detail recently by Messenger and Ash [1]. In addition, there are other specialized applications that may include narrowly defined radiation requirements, such as nuclear power stations, nuclear waste disposal site monitors, high-altitude avionics, and medical radiation treatments. We conclude this section with a brief discussion of the effectiveness of radiation shielding.

A. The Natural Space Radiation Environment

The radiation environment in space depends strongly on location, and is composed of a variety of particles with widely varying energies and states of ionization. Thus, radiation requirements are driven in large part by the nature and trajectory of the mission. For Earth-orbiting systems, such as communications satellites, the primary sources of radiation are electrons and protons trapped by the Earth's magnetosphere, as shown in the highly simplified diagram in Figure 10-1. These regions of trapped electrons and protons, called the Van Allen belts and discovered in 1958 by Explorer 1, are significant between the altitudes of approximately 1000 km and 32,000 km. Their extent is greater than this, but the particle flux levels drop rapidly outside this altitude range. As indicated in Figure 10-1, the altitude distributions of electrons and protons are significantly different. The distribution of electrons, whose energies reach a maximum of about 7 MeV, shows two altitude peaks at about 4000 km and 24,000 km, giving rise to

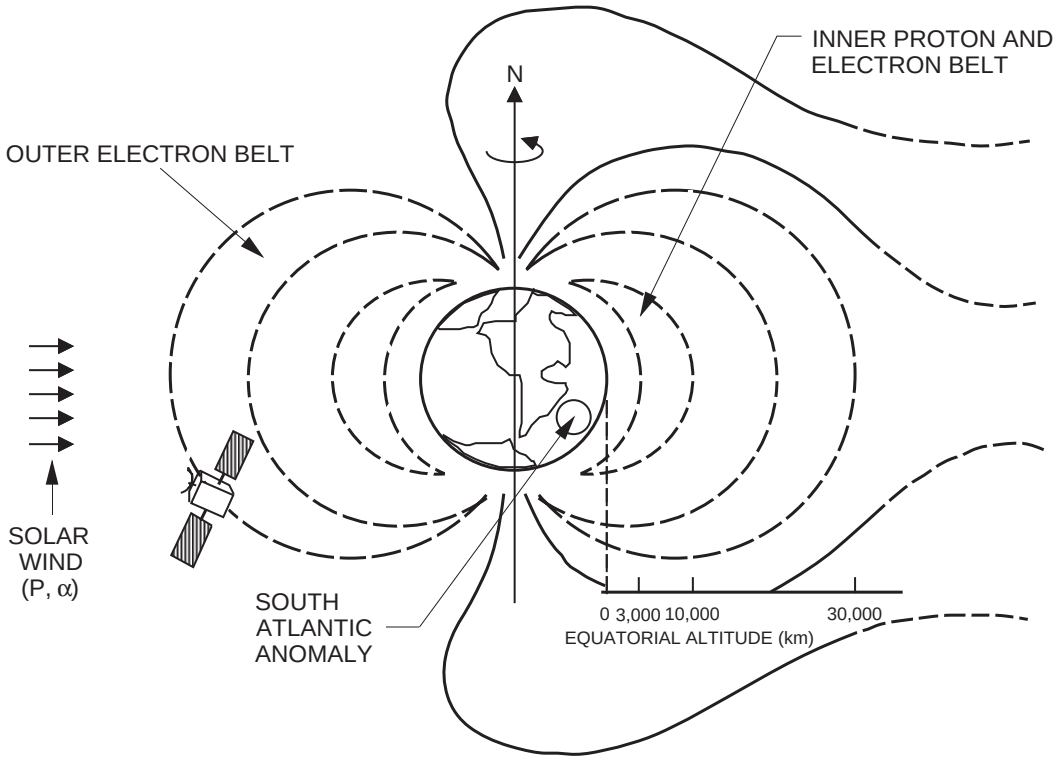

Figure 10-1. Schematic diagram of the Earth's Van Allen radiation belts formed by the Earth's magnetosphere.

the two belts shown in Figure 10-1 with a relatively unpopulated "slot" between the inner and outer electron belts. Protons are restricted to the inner belt, but their energies can be much higher than those of electrons—in excess of several hundred MeV. For both electrons and protons, the higher energy particles are concentrated at lower altitudes. At the lower energies, particle fluxes can exceed 1×10^8 electrons or protons per cm^2 per day.

Although the simple diagram in Figure 10-1 suggests that the belts are relatively symmetric, there are important exceptions to this overall symmetry. For example, at the Earth's poles, the outer electron belt extends downward to much lower altitudes. These "horns" in the belts cause a strong dependence of the particle flux at a given altitude on the angle of inclination. Another very important distortion is caused by the fact that the dipole axis of the Earth's geomagnetic field is offset from the Earth's axis of rotation by about 11 deg and is displaced by 500 km toward the Western Pacific. The result is that, off the coast of Brazil, the Van Allen belts reach down into the upper part of the atmosphere so that satellites at low Earth orbit (LEO) receive significant exposure to radiation over this region, called the South Atlantic Anomaly (SAA). Finally, the Sun also has a strong effect on the shape of the Earth's magnetosphere. The solar wind causes a "bow wave" and a "wake" in the antisolar direction that is similar to a boat moving through water and results in the extension of the magnetosphere to much greater distances from the Earth, as indicated schematically in Figure 10-1.

The characteristics of the Van Allen belts briefly summarized above result in dose-rate distributions for electrons like those shown in Figure 10-2 for an altitude of

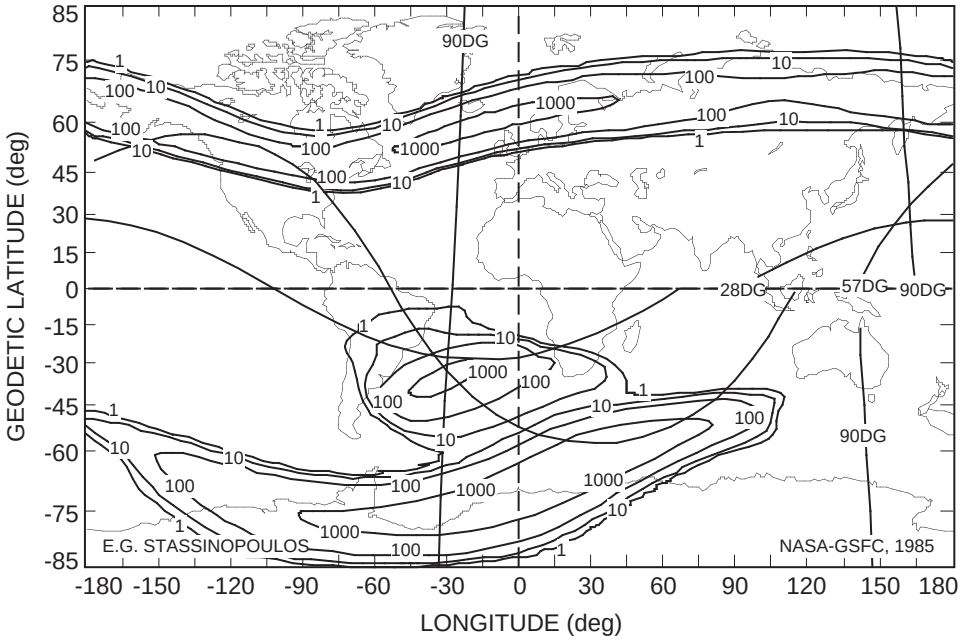

Figure 10-2. World map contours of electron dose at an altitude of 500 km. For the contours, 100 is equal to approximately 8.6 rads(Si) per day. (From [3]; ©1994 IEEE.)

500 km behind a spherical shield with thickness of 0.2 gm/cm^2 (equal to approximately 30 mils for Al) [2,3]. The dose rate is given in rads(Si) per unit time, where a rad is a measure of absorbed ionizing energy and is equal to 100 ergs/gm of the absorbing material (Si in this case). Note the clear delineation of the SAA by the isodose-rate curves, and that the dose rate is greater near the poles. Note also that the low inclination angle orbits do not pass through the higher dose-rate zones near the poles. It is important to emphasize that these dose rates are behind an Al shield because of the presence of very high fluxes of low energy (< 0.1 MeV) electrons and protons that can drive the dose to much larger values when no shielding is present.

Solar flares are another important source of ionizing radiation particles, particularly protons. Electrons, alpha particles, and heavier ions are also emitted, but at much lower fluxes than the high energy protons. The first indication that a solar flare has occurred is the arrival near Earth of a burst of X-rays. After about 10 min, highly energetic protons begin to arrive and significant fluxes of protons can last for a few hours to a day or so. As shown in Figure 10-3, the general sunspot activity follows an approximate 11-year cycle, although not all of this sunspot activity results in significant solar flares. Note that large flare occurrences are concentrated during solar max periods. The very large flare that occurred in August 1972 has become a benchmark against which conservative estimates of solar flare proton fluxes are made. As indicated in Figure 10-3 by the energy partition, solar flares can vary significantly in their proton energy spectrum, with some exhibiting much harder spectra than others. The inability to predict when a solar flare will occur and what its particle and energy content will be forces space system designers to use conservatively large estimates of potential flare activity.

The interaction of particles ejected by the Sun with the Earth's magnetosphere results in complex and sometimes unexpected dynamic behavior of the radiation flux [3].

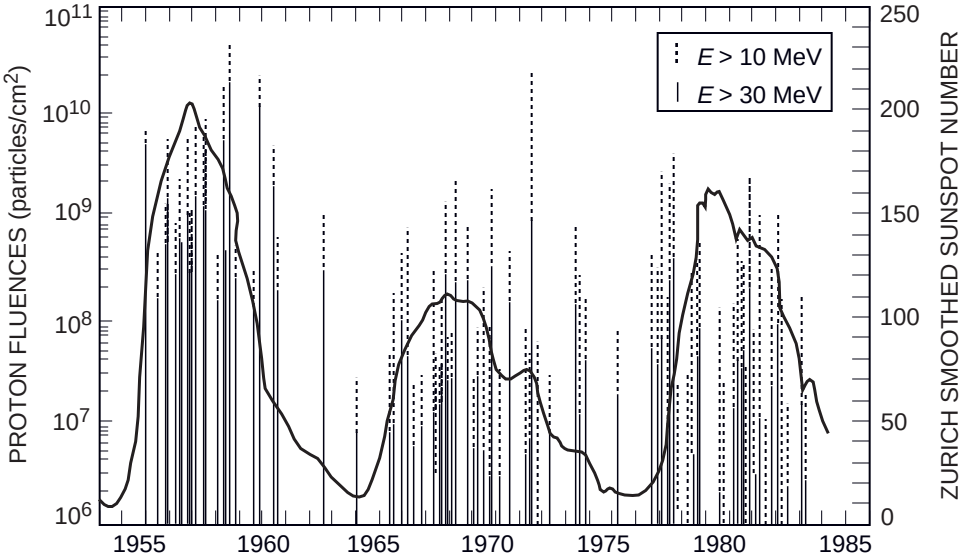

Figure 10-3. Sunspot activity and solar flare events for solar cycles 19, 20, and 21. Note the very large flare in 1972 that was a benchmark event. (From [4]; ©J. Geophys. Res., 1988.)

For example, one might expect that radiation fluxes would in general be greater around periods of solar max as implied by Figure 10-3. However, at low altitudes, the proton fluxes are lower at solar max because of an increase in the density of the atmosphere at altitudes of 200 to 1000 km; the greater density is caused by increased solar energy output at solar max. This density increase results in a depletion of those trapped particles that approach minimum altitudes in the belts. At the higher altitudes of geosynchronous orbits (GEOs), for example, complex dynamic fluctuations are also observed because of the influence of the Sun on the magnetosphere's properties. We also note that for low altitudes and angles of inclination, the magnetosphere provides a shielding effect on solar particles, but that for polar orbits, the flare protons can be funneled down to low altitudes, again emphasizing the dependence of radiation exposure on the angle of inclination for orbiting satellites.

The third important source of radiation in the natural space environment is galactic cosmic rays (GCRs), consisting of about 85% protons, approximately 14% alpha particles, and about 1% heavy nuclei [3]. These particles originate outside the solar system and are believed to be distributed uniformly throughout the galaxy. GCRs can be very energetic, reaching energies as high as 10 GeV/nucleon. While ions as heavy as uranium have been observed, the incidence of ions with atomic numbers greater than iron is rare. The distribution of GCR ions as a function of energy is shown in Figure 10-4. The heavier ions like Fe are present in much smaller densities. However, because the heavy ions deposit so much energy as they pass through a semiconductor device circuit, they can be more damaging overall even though they are much rarer in occurrence.

The energy and spatial distributions of GCR particles vary with location of the spacecraft. For interplanetary missions, typical of NASA projects, the energy spectrum is undegraded and the GCR flux is omnidirectional. However, for low-inclination-angle LEO satellites, the Earth's magnetosphere provides partial shielding of the GCR flux. This effect is shown in Figure 10-5 for Si ions as a function of their energy and the angle of orbit inclination at an altitude of 600 km [3,5]. Note that at small angles, the low-energy portion of the spectrum is strongly attenuated, while at large polar angles

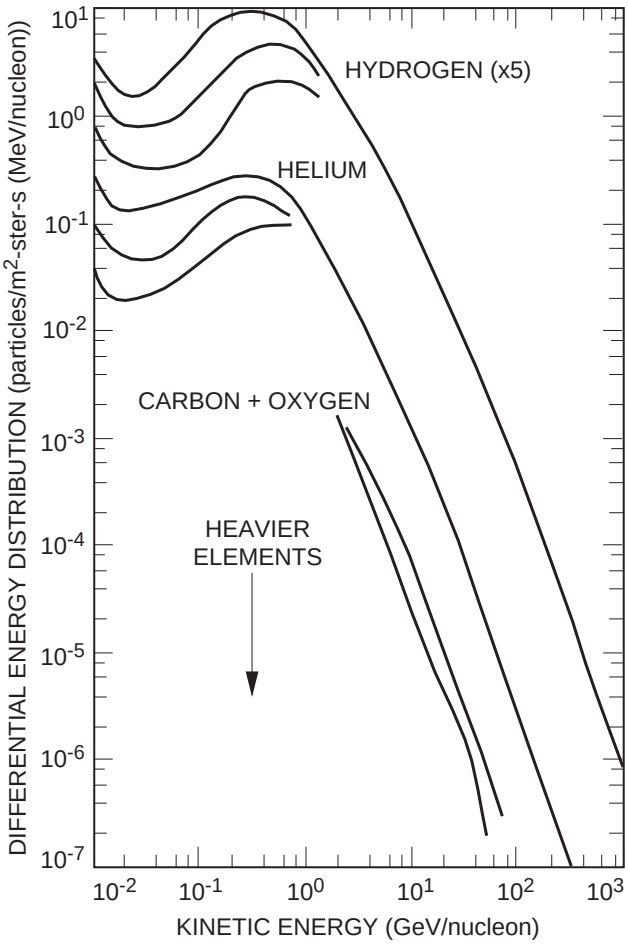

Figure 10-4. Distribution in energy and abundance of various galactic cosmic ray particles. (From [5]; ©1988 IEEE.)

(90 deg), there is a much smaller reduction in the flux of Si ions due to shielding by the magnetosphere.

While there is some uncertainty in calculating the expected radiation environment for a particular mission, primarily because of solar flares, sophisticated models and calculational codes have been in place for some time, and these are more or less continuously improved upon and updated [5–8]. Thus, it has become fairly standard practice to calculate environmental predictions of expected dose and heavy ion flux for given missions. The same is true for shielding calculations, which also can be quite complex for a relatively complicated spacecraft structure.

B. Other Radiation Sources

Military space assets are often designed to withstand not only the natural space environment, but also the added components due to detonation of nearby nuclear weapons. For this scenario, in addition to GCR ions, solar flare particles, and the Van

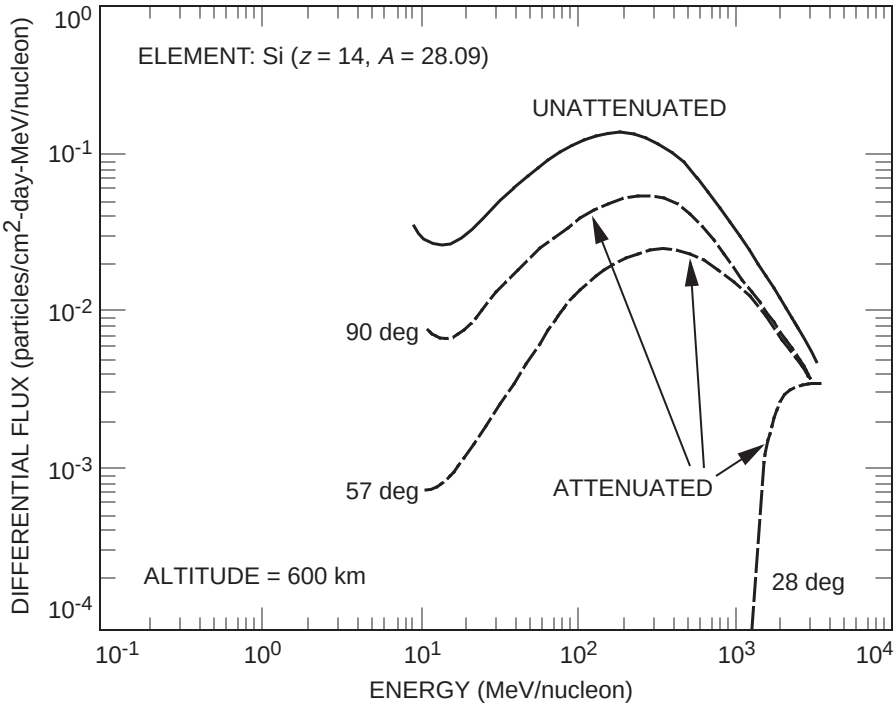

Figure 10-5. Attenuation of galactic cosmic ray Si ions by the Earth's magnetosphere at an altitude of 600 km for various angles of inclination. (From [5]; ©1988 IEEE.)

Allen belt electrons and protons, one must add large fluxes of neutrons, high-energy gamma rays and electrons, low-energy X-rays, and prompt bursts of gamma rays at very high dose rates. Thus, the military radiation environment is very difficult and demanding, particularly the prompt gamma dose, which is typically in the range 10^9 rad(Si)/s to 10^{12} rad(Si)/s.

In specialized cases, other man-made sources of radiation can be important. For interplanetary missions that extend to large distances from the Sun, as for the Galileo mission to Jupiter, nuclear sources are often used to provide electrical power to the spacecraft and its instruments. Radioisotopic thermoelectric generators (RTGs) generate enough gamma rays and neutrons to affect the performance of microelectronic circuits on the spacecraft near the RTGs. In the future, if other nuclear power sources, such as spaceborne nuclear reactors, come into being, there will be similar concerns for the exposure of electronics located near the nuclear power source.

When high-energy radiation passes through a material such as a radiation shield, nuclear interactions occur with nuclei of the material resulting in the emission of secondary radiation in the form of a continuous energy spectrum of energetic photons (Bremsstrahlung), gamma rays, electrons, alpha particles, and neutrons. These secondary particles can also cause damage to electronic circuits in the same manner as the primary radiation. Thus, in determining the total radiation flux that reaches the microelectronic devices and circuits, secondary radiation must be taken into account, especially if thick, high-Z (high atomic number) materials are present.

C. Radiation Shielding

The effectiveness of radiation shielding as a method of protecting electronics is often dependent on the circuit and its packaging or board configuration. However, some general comments concerning shielding are appropriate at this point. We have already noted that the various sources of radiation in the natural space environment contain significant low-energy components. Thus, even a nominal shield (less than 100-mil Al), as typically provided by the spacecraft structure and electronics boxes, can reduce the dose by several orders of magnitude. This effect is easily seen in Figure 10-6, which shows differential trapped proton flux as a function of energy and Al shield thickness for an orbit at 500 km altitude and an angle of inclination of 60 deg [5]. Very often, one of the difficulties in defining a total-dose radiation requirement with any precision for a specific mission results from variations in shielding with location in the spacecraft. Usually a nominal total dose—for example, 100 krad(Si) for the Cassini mission—is defined by the expected mission trajectory and the environment encountered; specific doses are then calculated for particular positions within the spacecraft. The impetus for following this procedure is especially strong when designers wish to use parts that do not meet the nominal requirement.

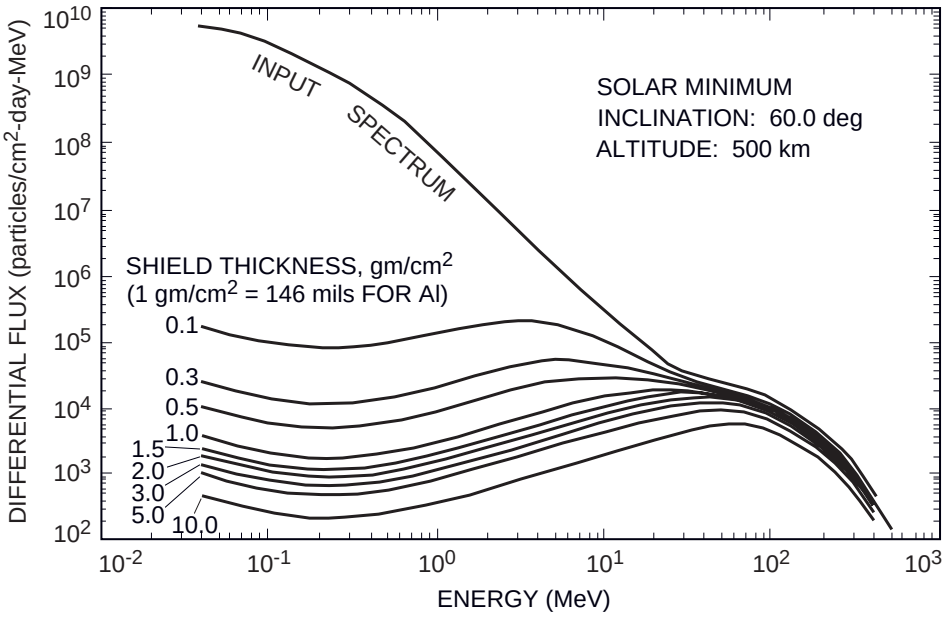

Figure 10-6. Van Allen belt trapped proton spectra emerging from spherical shields of various thicknesses for a 500-km orbit at 60-deg inclination and solar minimum. (From [5]; ©1988 IEEE.)

With greater use of commercial electronic parts in space, there are often cases when the shielding provided by the spacecraft structure is insufficient, and alternative radiation-resistant parts are not available. In such cases, spot shielding of the part is appropriate, including integrating shield material (high-Z elements like tantalum or tungsten) into the part package itself, a technique often referred to as "RadPak." As noted above, the implementation of these various shielding schemes to reduce the expected total dose is aided by the fact that shielding calculations used to determine the effect of a material on the flux and energy spectra of various types of radiation are well established. These calculations also take into account the production of secondary radiation.

While shielding can facilitate the use of "soft" parts in many cases, it is important to realize that shielding is not always effective, and can even make the situation worse. As a rule of thumb, shielding is most effective in reducing the low to moderate energy component of ionizing radiation, that is, electrons and protons. For very-high-energy radiation, such as gamma rays and GCR ions, shielding is not particularly effective, and can even be detrimental. This is partly due to the production of secondary radiation in the shield material, and also because the energy loss per unit length in the electronic part can increase with decreasing particle energy. The production of secondary radiation results in the asymptotic behavior of shielding effectiveness. In other words, the first thin layer is much more effective in reducing radiation than the additional thicknesses of shielding, as shown in Figure 10-6. Thus, beyond a few tens of mils of Al-equivalent shielding, the weight penalty is often more important than the added benefit of the radiation shielding.

The effectiveness of shielding in reducing the overall amount of radiation impinging on spacecraft electronics causes a sharp distinction between the natural space environment and the nuclear weapon-enhanced environment [1]. As noted earlier, weapon detonation results in a burst of prompt, high-energy gamma rays and, somewhat later in time, a significant fluence of 14-MeV neutrons. Shielding is of little use in moderating either of these radiation threats. Similarly, it is difficult to shield against the neutrons and high-energy gamma rays continuously emitted by RTGs as a byproduct of the power generation process. For this reason, the RTGs on Cassini have proven to be a challenging radiation threat to nearby microelectronics on the spacecraft.

III. Radiation Effects in Semiconductor Devices

In this section, we very briefly review the salient features of the effects of radiation on semiconductor devices. More thorough discussions can be found in References [1,9–11], and in the yearly Short Courses on this topic presented and published by the IEEE Nuclear and Space Radiation Effects Conference. To introduce this subject, we focus on radiation effects in Si devices, particularly digital complementary metal-oxide semiconductor (CMOS) and analog bipolar. In addition to allowing us to briefly review traditional radiation effects, this focus will provide a baseline for our review of radiation effects in MMIC devices. For purposes of discussion, we designate three categories of radiation effects: (1) ionizing radiation effects, (2) displacement damage effects, and (3) single-particle or single-event effects (SEE).

A. Ionizing Radiation Effects

With the exception of neutrons, the various types of radiation making up the natural and weapon-enhanced environment—X-rays, gamma rays, electrons, protons, alpha particles and heavier ions—all deposit significant amounts of ionizing energy in semiconductor devices. In semiconductors and insulators, the absorbed ionizing energy manifests itself as electron-hole pairs that can separate, migrate through the material, and become trapped at certain locations, often resulting in an alteration of the properties of the device in which the energy was deposited. The fraction of the total generated charge, electrons and holes, that eventually becomes trapped is called the charge yield and depends on the structure and operating conditions of the device during radiation exposure, and also on the type of radiation and its energy. In many cases, nearly all the charge recombines or is collected at contacts in such a way that the ionizing radiation has

little effect on the device. As we will see, this is usually the case with III–V material-based technologies, such as laser diodes, LEDs, and MMIC devices.

In sharp contrast with the III–Vs, such as GaAs, perhaps the most widely known and widely studied [9] structure that exhibits a sensitivity to ionizing radiation is the silicon dioxide–silicon (SiO_2–Si) interface and its nearby regions, found in all Si CMOS devices, and also in Si bipolar circuits with oxide isolation. The vulnerability to ionizing radiation of digital CMOS circuits can be attributed almost entirely to oxides near Si interfaces in the structure of these circuits. In particular, metal-oxide semiconductor field effect transistor (MOSFET) gate oxides and field oxides used to isolate portions of the circuit from each other can cause large changes in device properties (MOSFET threshold voltage shift, increased leakage current, and degraded timing parameters) because of the creation and trapping of charge in these oxides. In addition, the imperfections located at the SiO_2–Si interface result in the radiation-induced growth of defects in the form of "interface states" within the Si near the interface that can lead to different failure mechanisms than those due to the trapped charge in the oxides. Whether device degradation and failure will be due to oxide-trapped charge or interface state effects is determined in a very complex manner by the interplay of a variety of parameters, including type of radiation, dose rate, temperature, magnitude and sign of bias applied during irradiation, oxide quality and thickness, and post-oxide growth processing temperatures. The complicated nature of the radiation response of CMOS devices and circuits, and their importance to space and defense systems, has led to many years of study of radiation effects in MOS-based devices, and the publication of an enormous number of papers on this subject [12]. Shown in Figure 10-7 is a summary of radiation hardness levels for various MOSFET-based integrated circuit technologies [13]. As a rough rule of thumb, unhardened commercial technologies exhibit failure doses from a few krad(Si) to a few tens of krad(Si), "radiation tolerant" technologies are in the range of 100 krad(Si), and intentionally hardened technologies can be in excess of 1 Mrad(Si). In the future, scaling effects (reduced feature sizes) will lead to greater gate-oxide hardness because these oxides will be thinner, but continuing problems with field oxides, which will result in current leakage within the circuit.

Although the sensitivity of Si bipolar-technology digital circuits can be similar to that of digital CMOS because, as noted above, they also employ oxide isolation techniques, bipolar circuits do not contain sensitive gate oxides directly over carrier channels and are thus not sensitive to gate-oxide degradation mechanisms. The generally less radiation-sensitive nature of bipolar technologies can be seen by comparing Figure 10-8 [13] for bipolar circuits with Figure 10-7. Note that this bar chart also contains a hardness level for GaAs digital circuits, and that this level is greater than that for all the Si technologies shown because of the absence of SiO_2 oxides in the GaAs circuits.

In the case of Si bipolar linear circuits, radiation susceptibilities can often be surprisingly low, in the range of a few tens of krad(Si). Devices such as operational amplifiers, comparators and voltage references can exhibit radiation sensitivities in the form of changes in offset voltage, offset current, bias current, and open loop voltage gain. More recently, state-of-the-art bipolar linear circuits have shown an unusual dose-rate dependence: in contrast with digital CMOS, they are more sensitive at low dose rates (less than about 1 rad(Si)/s) than at moderate to high dose rates [14]. Although the exact mechanism for this enhanced low-dose-rate effect has not yet been explained, it appears to be connected with the dynamics of charge motion in thick isolation oxides with low electric fields present [15].

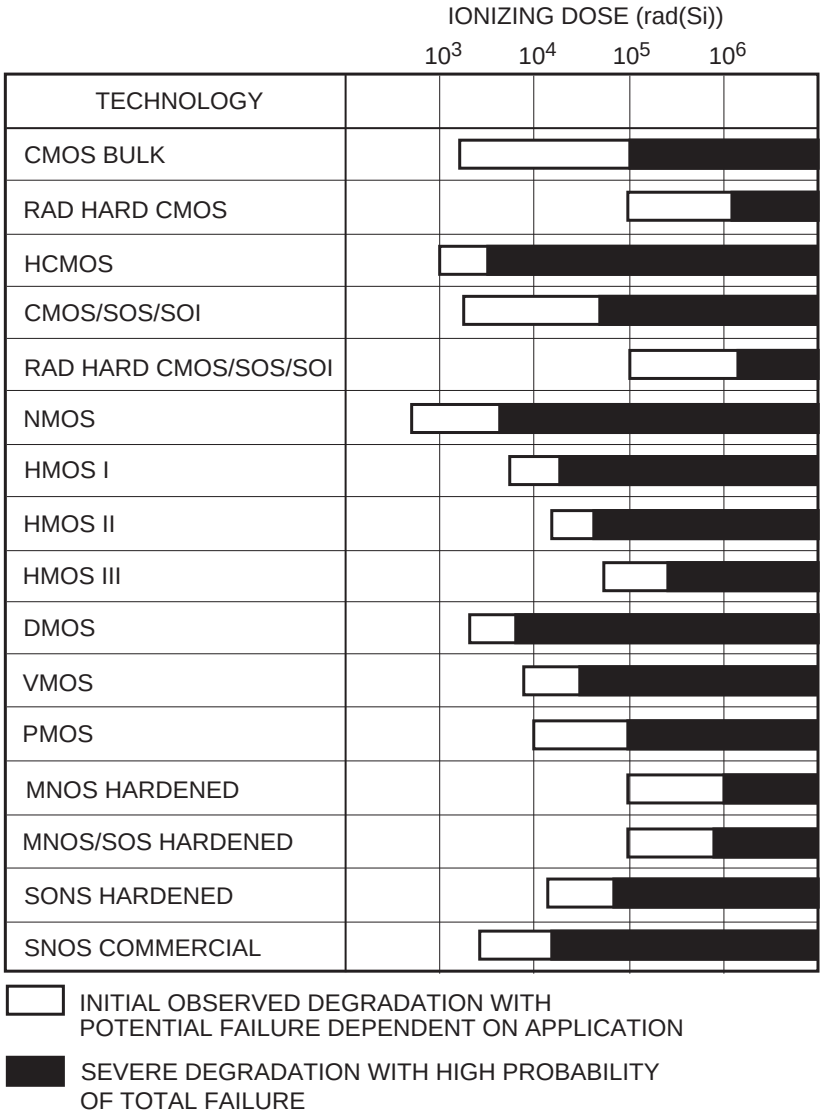

Figure 10-7. Ionizing-dose failure levels for MOSFET integrated circuits. (From [13].)

To provide a broader comparison of total-ionizing-dose hardness levels, Figure 10-9 [13] includes a variety of different technologies including those discussed briefly above, and also Si-discrete devices, GaAs devices, charge coupled devices (CCDs), crystal resonators, and optical fibers. It is interesting to note that in this bar chart, created in 1990, Si bipolar transistors do not show failure until a dose level of about 1 Mrad(Si) is reached. However, recent testing of transistors at JPL for the Cassini mission has indicated significant degradation at tens of krad(Si). The reason for this is presumably that performance "improvements" in the transistors (e.g., an ability to operate over a wider collector current range) have increased the radiation vulnerability. In fact, performance enhancements in Si technologies have often led to increased radiation sensitivity. Finally, we note that the GaAs circuits in Figure 10-9 are among the hardest shown in this bar chart.

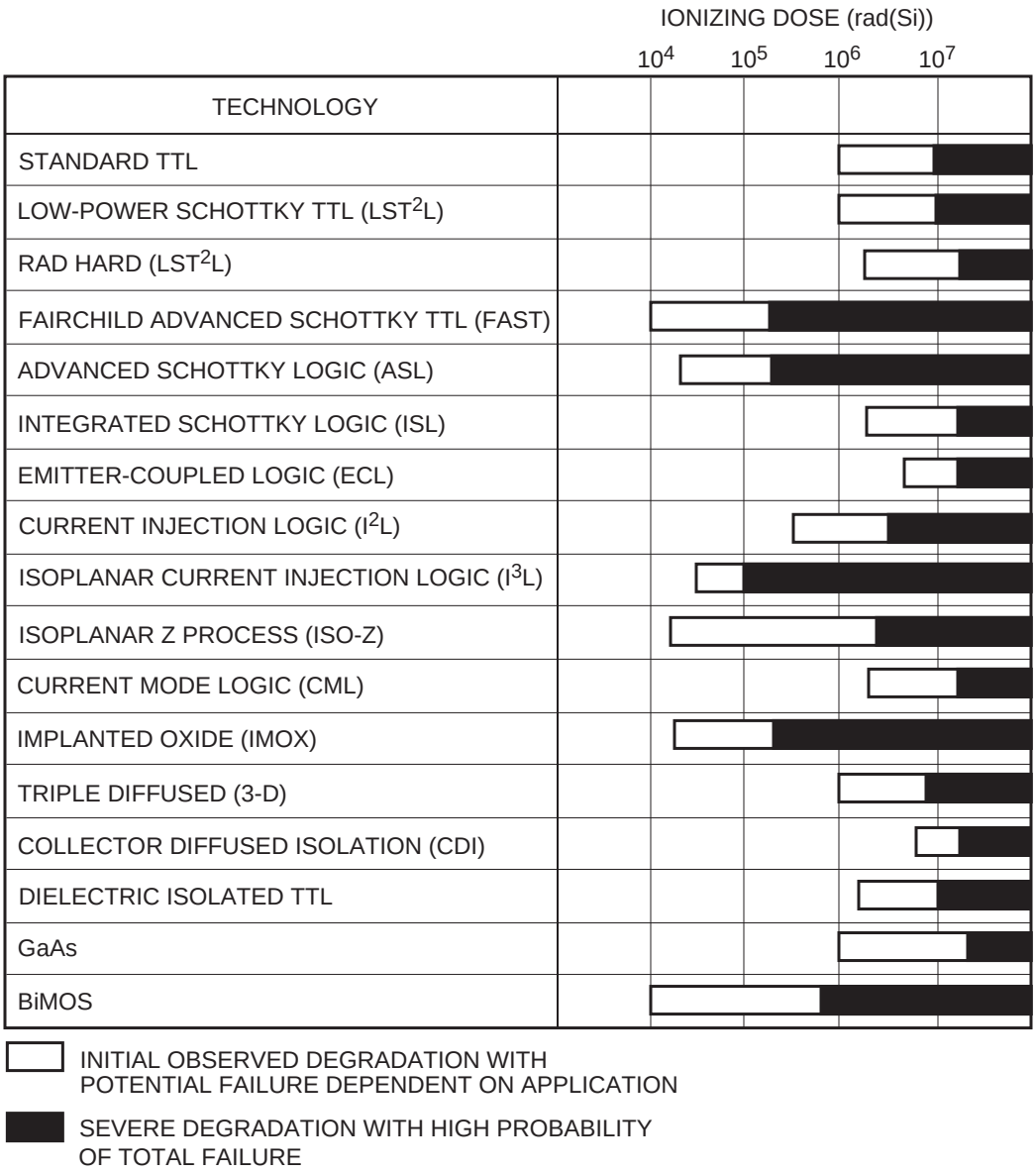

Figure 10-8. Ionizing-dose failure levels for bipolar integrated circuits. (From [13].)

Thus far, our discussion of ionizing radiation effects has been restricted to the steady cumulative effects observed after moderate dose-rate irradiations, so-called total-ionizing-dose (TID) effects. While room temperature annealing of trapped hole charge is usually observed after such irradiations, it occurs slowly and is viewed as "permanent" in nature relative to transient, high-dose-rate effects. Even though prompt dose-rate effects in the range 10^8 rad(Si)/s to 10^{12} rad(Si)/s are not of direct interest to NASA and commercial space applications because they only occur for the nuclear weapon-enhanced environment, it is worthwhile to very briefly review these high-dose-rate effects.

When a semiconductor device or circuit is exposed to prompt, high-dose-rate irradiation, very large electron-hole densities are created throughout semiconductor and insulator materials. The eventual impact of these high excess carrier densities on the operation of the circuit depends on the fraction of the excess carriers collected as photocurrent at junctions in the circuit structure, and on the effect of transient

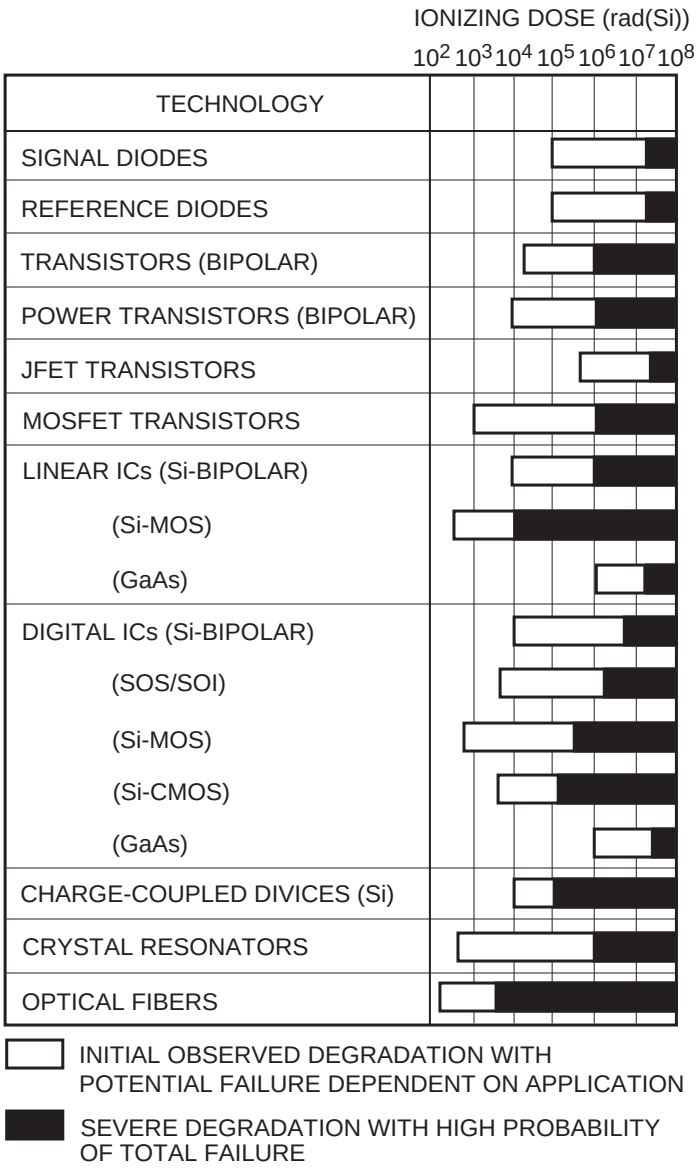

Figure 10-9. Ionizing-dose failure levels for discrete, linear, and digital device families. (From [13].)

photocurrents on circuit function. Realizing that a pulse of magnitude 10^9 rad(Si)/s can create electron-hole densities as large as $10^{18}/cm^3$, well above the doping level in many semiconductor devices, it is not hard to understand that prompt bursts of penetrating radiation in the range 10^8 rad(Si)/s to 10^{12} rad(Si)/s can have a profound effect on circuit operation. Because such large excess carrier densities can overwhelm normal PN junctions and cause collapse of electric fields, unexpected effects due to large current flows in the circuit can occur, and sophisticated computer codes have been developed to predict circuit behavior under these extreme conditions [1,10,11]. The key structures in a circuit are reverse-biased PN junctions because the wide depletion layers associated with these junctions can collect large fractions of prompt dose-rate-generated carriers resulting in large transient photocurrents. The transient photocurrents produced in a variety of diode types are shown in Figure 10-10 [1]. Note that there is a wide variation in photocurrent magnitudes due to the different volumes in which carriers are generated and

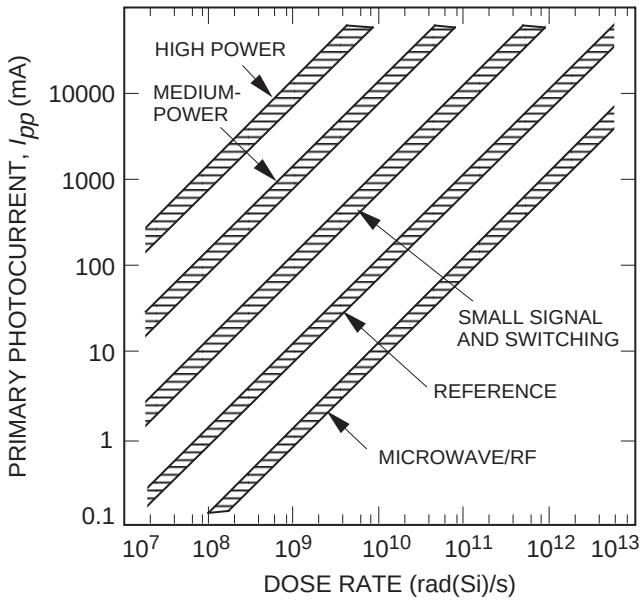

Figure 10-10. Primary photocurrent magnitudes generated by prompt dose-rate irradiations in various types of diodes. (From [1].)

the extent of the depletion layers in each type of device. Microwave devices, because of their small size, are on the lower end of the scale in Figure 10-10, while power devices exhibit the largest currents because of large junction areas.

Prompt, transient ionizing radiation at high dose rates causes two principal classes of detrimental effects in circuits: dose-rate upset, and dose-rate burnout and latchup, both potentially catastrophic effects. Each of these effects has several variations depending on the type of circuit and the conditions of exposure. Examples of dose-rate upset include [10] (1) memory cell upset in which the logic state of a cell is changed, (2) output voltage upset, (3) write mode address upset in a SRAM, and (4) pushout or SRAM access time delay. For large photocurrent transients, the effects can be more catastrophic: burnout of junctions and metal conductors, and rupture of dielectric elements. Dose-rate latchup can also be a catastrophic effect if the power supply can sustain a large latchup holding current until device destruction occurs. Latchup is similar to the switching of a silicon-controlled rectifier (SCR) in which the transient causes the device to enter a self-sustaining low-voltage, high-current state. The power to the device or circuit must be cycled to remove the latchup condition. In a CMOS circuit, latchup is initiated within two parasitic bipolar transistors, one vertical the other horizontal, for which the product of the gains of both transistors is greater than one. The susceptibility of a variety of device and circuit types to upset and latchup is shown in Figures 10-11 and 10-12 [13]. Note that GaAs digital and linear ICs are shown in Figure 10-12 and that their susceptibility to these effects is somewhat less, but still comparable to Si circuits.

A variety of techniques have been developed to mitigate transient, high-dose-rate-induced upset and latchup in Si electronic circuits [1,10,11]. These include dielectric isolation of circuit components, design and layout modifications to minimize photocurrent generation, growth of epitaxial layers on heavily doped substrates to avoid latchup, pulse detection and circuit clamping, current limiting resistors so that latchup holding currents cannot be sustained, use of alternative substrate materials such as

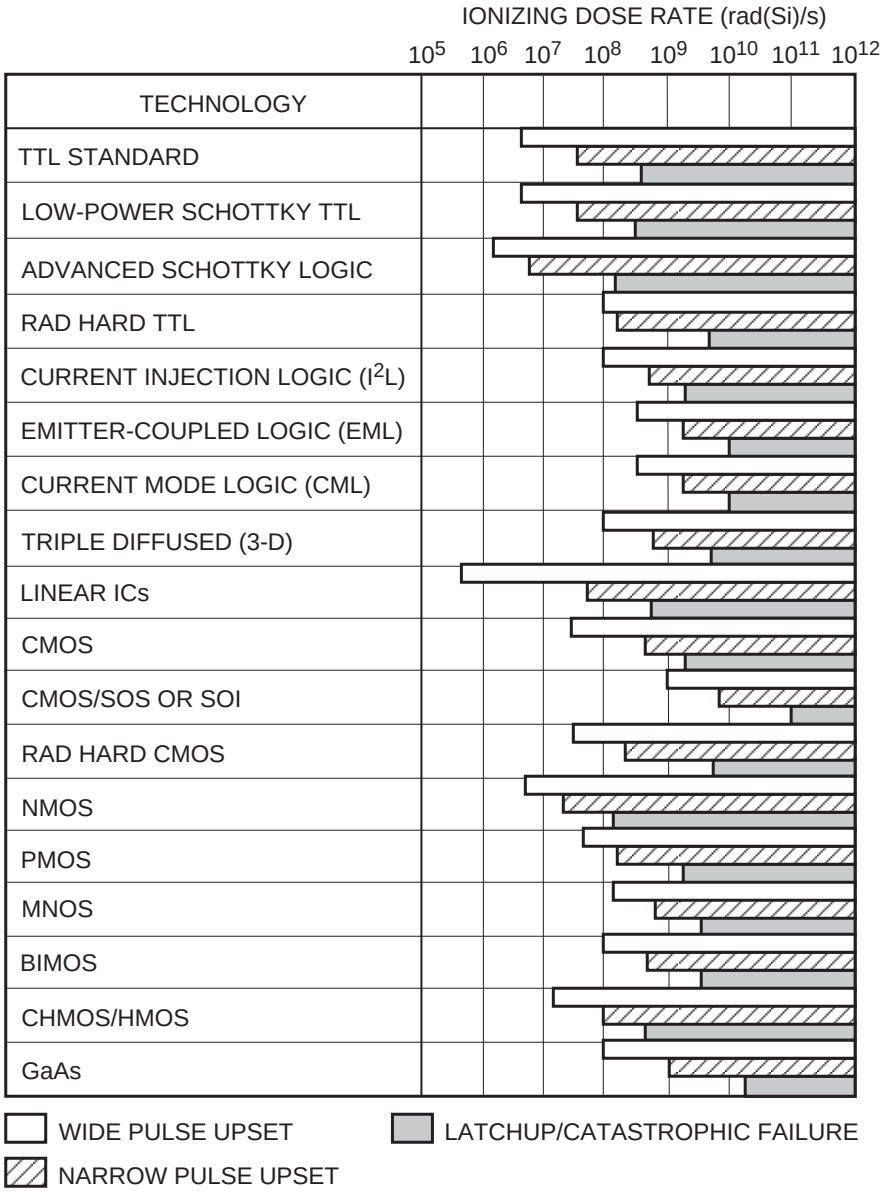

Figure 10-11. Prompt ionizing dose-rate hardness levels for bipolar and MOS integrated circuit families. (From [13.])

silicon-on-insulator (SOI) or silicon-on-sapphire (SOS), and the avoidance of high-gain circuits and devices with large collection volumes.

B. Displacement Damage Effects

Displacement damage effects occur in bulk semiconductor materials because of scattering interactions of heavy particles, such as protons and neutrons, with the atoms of the semiconductor lattice. In the initial scattering event, the bombarding particle displaces an atom from its lattice site, and this “primary knock-on” produces an additional cascade of displacements, the magnitude of which depends on the amount of kinetic energy transferred to the primary knock-on by the proton or neutron. The

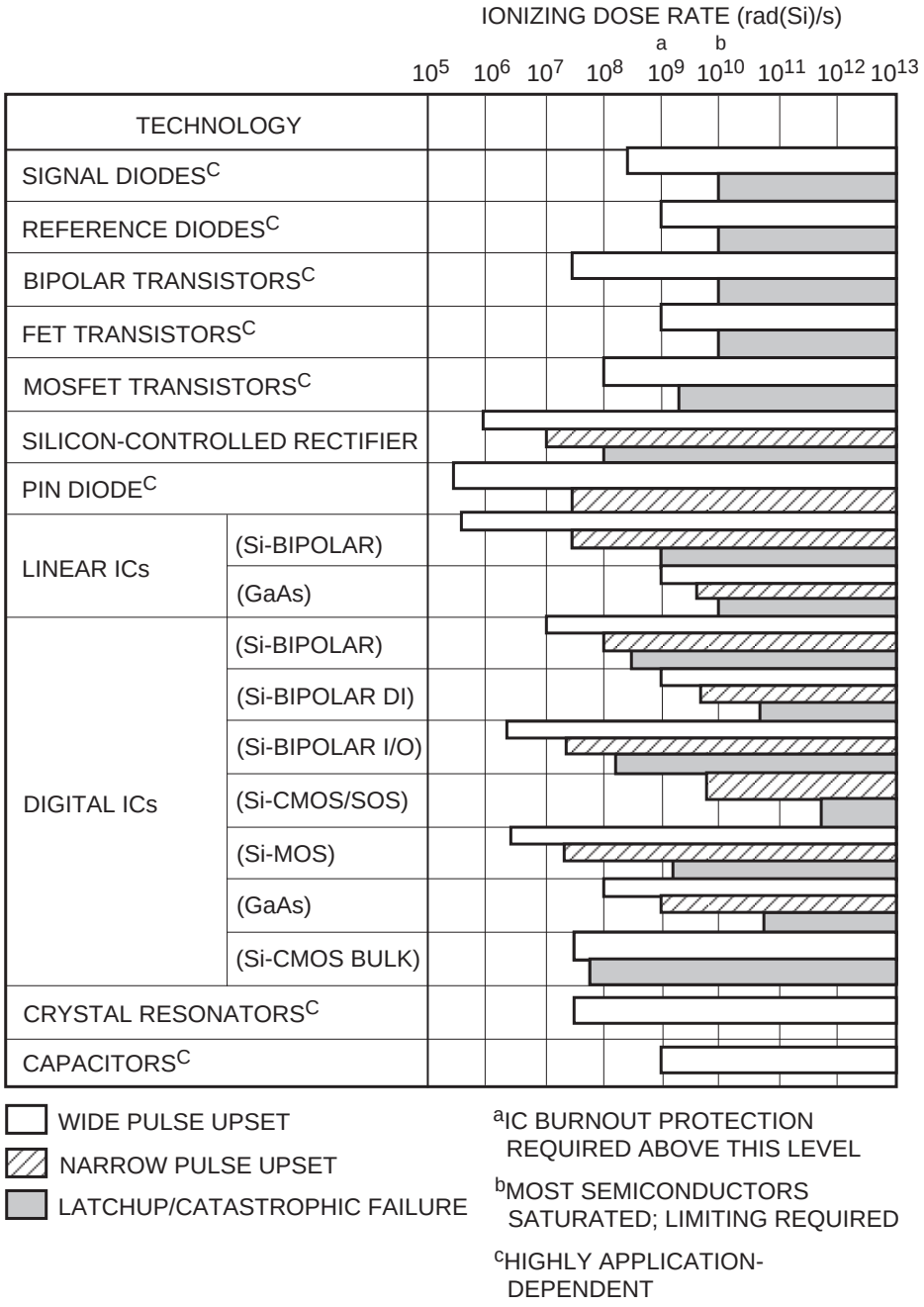

Figure 10-12. Prompt ionizing dose-rate hardness levels for discrete device families. (From [13.])

production of displacements is greatest near the end of the track of the energetic particle, whether it is a primary or secondary knock-on or the irradiating particle. The distribution of displaced atoms differs somewhat between neutrons and protons because the primary interaction mechanisms are different: protons scatter primarily by Rutherford scattering, which involves relatively low energy transfer (forward scattering), while neutrons interact primarily by elastic, "billiard ball" scattering with high energy transfer. In any case, the end result is that defects, interstitials, and vacancies are created in the

semiconductor and can become trapped, or migrate and combine with other defects and impurity/dopant atoms to form complex defects (divacancy, oxygen vacancy, and phosphorus vacancy in Si, with similar types in GaAs) with energy levels within the forbidden gap that act as carrier traps and recombination centers. In this manner, displacement damage can alter the electrical and optical properties of a semiconductor device or circuit.

Just as there are significant differences in the manner in which displacement damage forms relative to the ionization-induced damage discussed above, there are correspondingly large differences in the ways that the two types of damage affect device and circuit properties. While ionization damage primarily affects oxides and interfaces within the circuit, displacement damage affects the bulk properties of the semiconductor itself. The radiation-induced defect levels reduce the minority carrier lifetime and then, at higher defect concentrations, they cause carrier removal and reduce the majority carrier concentration. Thus, the types of devices and circuits that are most sensitive to displacement damage are those that depend on large values of minority carrier lifetime for satisfactory performance: bipolar transistors (except for very-high-speed switching transistors), linear bipolar circuits, BiCMOS circuits, phototransistors, LEDs, and solar cells. Since MOSFETs are majority carrier devices that are usually relatively heavily doped, they are not very sensitive to displacement damage because large concentrations of radiation-induced defects must be present in order to cause significant majority carrier removal to occur. Thus, Si CMOS circuits are not particularly susceptible to displacement damage.

In discussing displacement damage, we have mentioned protons and neutrons as the two particles of interest in the radiation environment. However, it should be emphasized that other types of radiation, gamma rays, electrons and heavy ions, can also cause displacement damage. However, electrons, and especially gamma rays through the creation of Compton electrons in the material, cause lattice displacements at a relatively low rate. Thus, only the most sensitive devices, such as Si n-on-p solar cells with their very long minority electron lifetimes in the base region, will show significant degradation due to displacement damage from gamma rays and electrons.

From the NASA and commercial space applications perspective, protons are a particularly important threat not only with regard to displacement damage formation (neutrons are encountered only in special circumstances, as noted above), but also because they produce significant amounts of ionization damage effects. If one places a mixed signal device, such as an analog-to-digital converter (ADC) that contains both bipolar and MOS components (BiCMOS) in an environment dominated by large proton fluences, the radiation hardness assurance (RHA) problem becomes very challenging because of the variety of failure modes that can occur, and the dependency of these failures on a large number of parameters. For example, under one set of conditions, an ADC may fail due to displacement damage, while under another set of conditions, the degradation and failure may be dominated by ionization effects.

With regard to the threat posed by displacement damage effects, the military point of view can be significantly different from that of other space users. In the nuclear weapon-enhanced environment, neutrons are a greater threat than protons, and the neutron requirement will determine the extent of potential displacement damage effects. The susceptibility to neutrons of various types of discrete devices and integrated circuits is shown in Figures 10-13 and 10-14 [13]. Note that GaAs circuits are relatively hard to neutron irradiation because of their relatively short minority carrier lifetimes and high majority carrier concentrations.

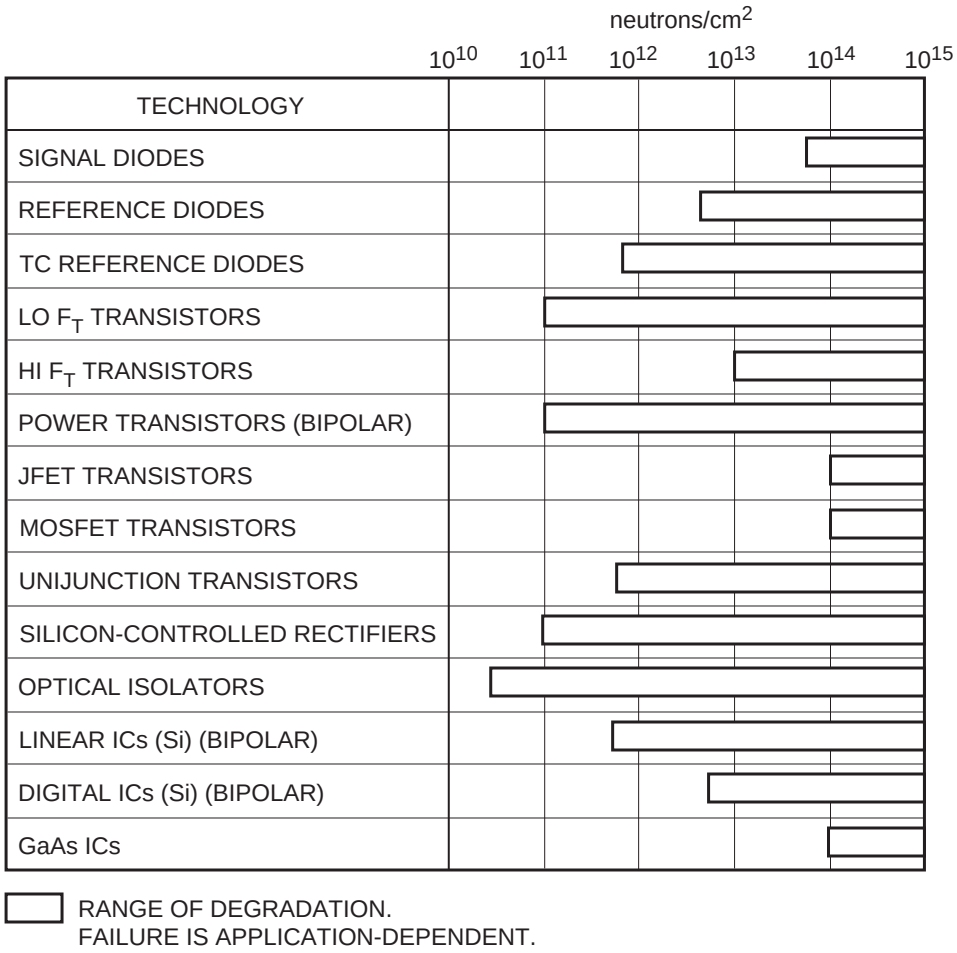

Figure 10-13. Neutron hardness levels for discrete devices. (From [13].)

C. Single Event Effects

As early as 1962 [16], it was predicted that when microelectronic feature sizes became small enough, upsets in circuits due to the interaction of GCR ions with devices on the circuit would be observed. While it took several years for single event upset (SEU) to be viewed as a real problem, the rapid acceleration of microcircuit miniaturization (scaling) in recent years has led to the discovery of several types of single event effects (SEE). These effects can be classified as either transient effects or as permanent effects. In some cases, such as single event burnout (SEB), single event latchup (SEL), and single event gate rupture (SEGR), the permanent effects can result in catastrophic destruction of the microcircuit.

In space applications, SEE are most often caused by energetic heavy ions making up the GCR spectrum because these ions deposit energy in the semiconductor material at high densities. Microcircuits that are particularly sensitive to SEE can also be upset by protons and alpha particles, even though their energy loss per unit length is significantly less than that of energetic heavy ions. A commonly used measure of the effectiveness of an ion in causing SEE is the linear energy transfer or LET, which is equal to the energy loss per unit length divided by the density of the semiconductor and has units of MeV-

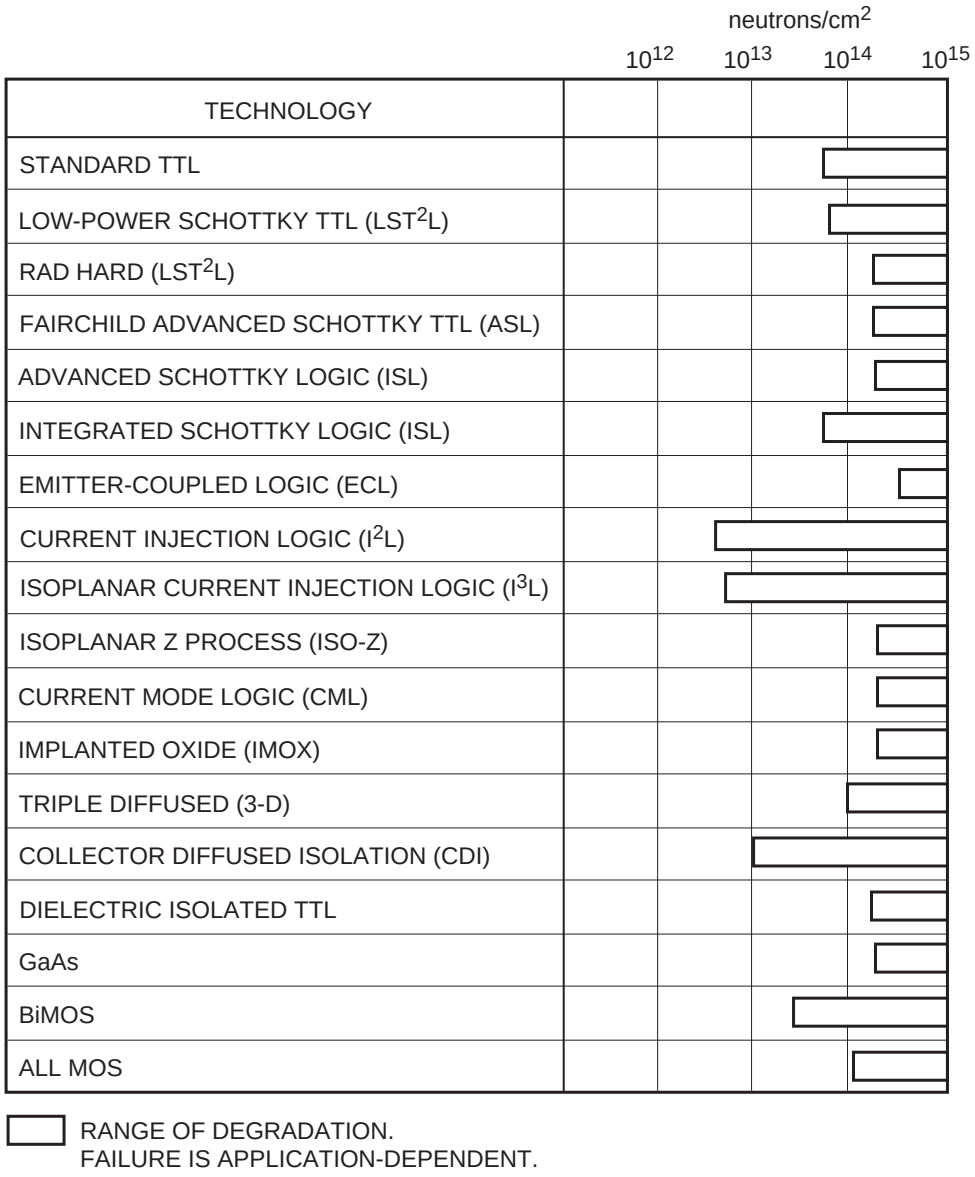

Figure 10-14. Neutron hardness levels for integrated circuit families. (From [13].)

cm^2/mg. LET values range from 1 to 10 MeV-cm^2/mg for protons of various energies to values approaching 100 MeV-cm^2/mg for heavy ions such as Xe with energies of several hundred MeV. It is important to emphasize that protons do not cause upsets directly; rather they produce nuclear interactions with target nuclei whose product nuclei have sufficient energy and mass to cause SEE.

Of the variety of single event effects, the earliest and best-known is single event upset (SEU), in which a heavy ion deposits enough energy in a bistable element to switch the logic state of that element. SEUs are easily observable in a memory that has not been hardened to single event upset. The process for upset of a memory cell is shown in Figure 10-15 for a six-transistor memory cell as one might find in a SRAM [17]. At the top of Figure 10-15, a cross-section of one inverter of the memory cell is shown along with an ion strike by a GCR particle on a sensitive node (junction of the OFF p-channel transistor) of the memory cell. Note that the ion is shown striking the cell at an angle

with the normal to the surface, which has the effect of increasing the path length through the sensitive charge collection region of the device. This increased path length is taken into account by defining an effective LET, LET_{eff}, which is equal to LET/cos θ, where θ is the angle with the normal. Thus, an ion hitting the surface at a 60-deg angle has a LET_{eff} twice that of the same ion striking normal to the surface.

The charge deposited and collected at one of the sensitive junctions shown in Figure 10-15 produces a transient current pulse that drives the hit inverter toward the opposite state (inverter on the left is driven to an output HI state as the gate voltages change due to the pulse). If the active transistor on the hit inverter does not annihilate the deposited charge and restore the gate voltage in time, the input state of the other inverter will be switched, leading to a change in output state that places the entire cell in the opposite logic state. Note that unlike a typical unhardened memory cell, the coupling lines between the two inverters making up the cell have resistors, R_G, in them. These resistors serve to slow down the feedback between the two inverters so that the gate voltage on the struck inverter can be restored before the altered charge state is communicated to the other inverter, thus hardening the cell against SEU. While this hardening technique is effective, it has the disadvantage of reducing the speed of the memory. In addition, the polysilicon resistors are quite temperature sensitive.

For a memory cell to be upset, the ion must deposit a minimum amount of charge, called the critical charge, Q_c, as it passes through the sensitive regions of the device. The critical charge is related to the LET threshold, LET_T, by the simple relationship,

$$Q_c = \frac{0.016 LET_T \rho l_c}{E_p}, pC \qquad (10\text{-}1)$$

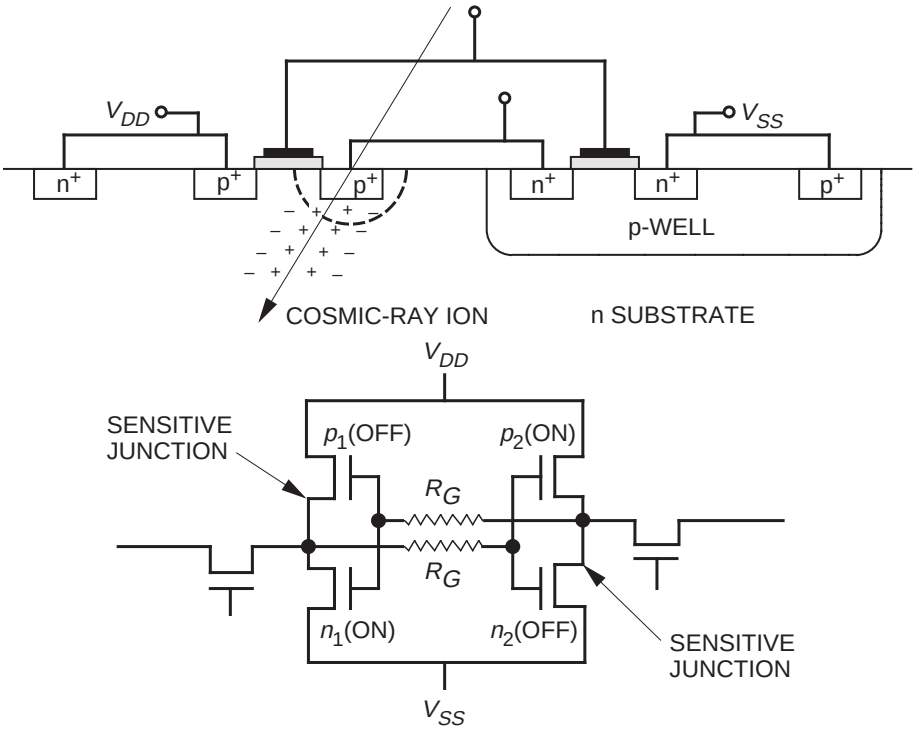

Figure 10-15. Single event upset in a typical SRAM memory cell. (From [17]; ©1985 IEEE)

where ρ is the material density (2.33 gm/cm^3 for Si and 5.32 gm/cm^3 for GaAs), l_c is the path length in μm through the sensitive region, and E_p is the minimum energy required to produce an electron-hole pair (3.6 eV in Si and 4.8 eV in GaAs). For a path length of l_c = 1 μm and a LET_T of 26 MeV-cm^2/mg, the so-called iron threshold above which the GCR particle abundance is much less, Q_c = 0.26 pC for Si and 0.46 pC for GaAs. Critical charge values of a few tenths of a picocoulomb are fairly typical for many technologies, suggesting a sensitivity to SEU in the LET range of a few tens of MeV-cm^2/mg. As one might expect, the Q_c for upset decreases as the feature size of an integrated circuit technology decreases, as shown in Figure 10-16 for a variety of technologies including GaAs [18]. Note that Figure 10-16 is somewhat dated and that feature sizes are now commonly below 1 μm. Thus, we can expect that the sensitivity to SEU effects may become more severe for certain microcircuits as technology scaling continues.

It is important to emphasize that the apparent simplicity of Equation (10-1) is deceptive, and it is given primarily as an illustrative rule of thumb. In particular, it is often very difficult to define the proper path length, l_c. The dynamics of charge flow during and immediately after an ion strike is still a subject of relatively intense scrutiny. This is partially because active device regions have become very small in the lateral directions, lending difficulty to defining and quantifying sensitive regions and the interaction of an ion striking the surface at a large angle. If the device is particularly sensitive to SEU, it can experience an event even if the ion strikes near but not within the active region because significant amounts of charge can be collected by diffusion. Another result of these scaling effects is that it continues to be a difficult challenge to

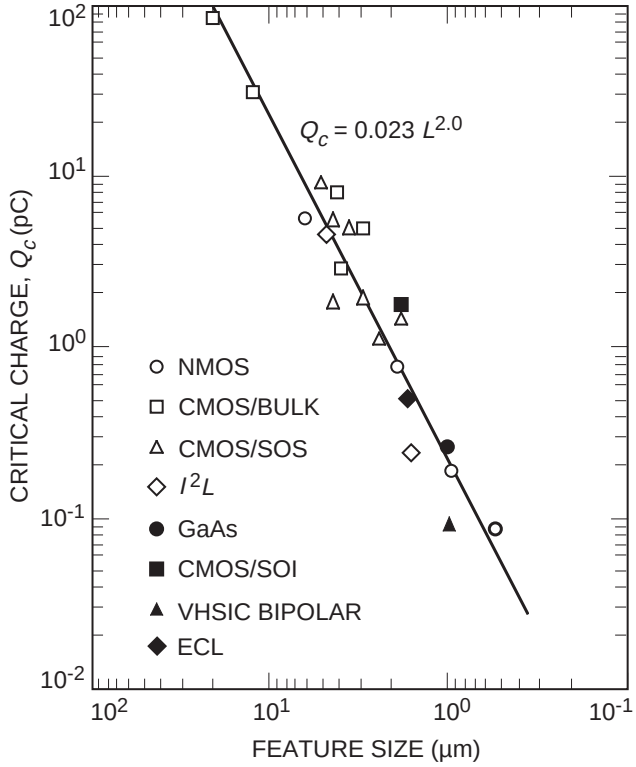

Figure 10-16. Dependence of critical charge for upset on feature size for various integrated circuit technologies. (From [18].)

relate SEU test data to the expected upset rate in space where particle strikes are omnidirectional.

One characteristic implied by Equation (10-1) is important to emphasize because it is generally true: single event effects tend to have a threshold as defined by the LET threshold, LET_T. This is particularly important because of the dramatically increasing abundance of lighter particles in the environment, as seen in Figure 10-4. Thus, if a circuit has a low enough LET_T, it will be sensitive to proton-induced SEU and the large concentrations of energetic protons in the environment can lead to high SEU rates.

In addition to the LET threshold, another important parameter that characterizes a part's SEU sensitivity is the SEU cross section. At the LET threshold, the most sensitive regions in a circuit begin to exhibit SEU, and the rate increases rapidly as the LET is increased and more regions in the circuit start to upset. In the ideal case, a point will be reached where all the sensitive regions are upsetting and the remainder of the chip is immune, so that the SEU rate saturates and the cross section approaches an asymptote referred to as the saturation cross section. Thus, for a "well-behaved" circuit, for which there are many exceptions, one can use LET_T and the saturation cross section as two parameters that fully characterize the SEU response of the circuit. It is interesting to note that for very sensitive circuits, where ions striking at oblique angles can cause multiple upsets and a significant amount of charge is collected by diffusion, the SEU cross section of the chip can be larger than the chip area! By way of summary, we provide Figure 10-17, which shows SEU susceptibilities of various technologies including GaAs [13].

A variety of other single event effects have been discovered, especially in recent years as scaling to smaller dimensions increases the general sensitivity of devices and integrated circuits to SEE. As we noted earlier, some of these effects can be catastrophic in nature. For example, circuit destruction can result from single event latchup (SEL), the single particle analogue to dose-rate latchup discussed earlier. Generally, the same techniques can be used to mitigate both types of radiation-induced latchup, and single event latchup is easier to cope with because the entire chip is not exposed as in the case of dose-rate latchup. Other important potentially catastrophic effects include singe event burnout (SEB) in power MOSFETs and single event gate rupture (SEGR) in MOSFETs. These effects require a combination of temporarily very large electric fields and local temperature excursions that result in severe device degradation.

IV. Radiation Testing

The key to performing effective radiation testing at ground-based facilities is to provide radiation test results that can be used to predict the circuit response in the actual space environment. While actual radiation flight experiments have been conducted and have provided valuable data about part response in the actual environment [19], these flight tests are very expensive and require long periods of time to implement. In addition, it is often difficult to sort out and precisely quantify the actual part radiation response because many parameters are changing at once in the space environment, and one has a limited ability to control and vary specific parameters. Thus, the principal burden of establishing radiation hardness assurance (RHA) must be placed on accurate, well-controlled laboratory radiation tests.

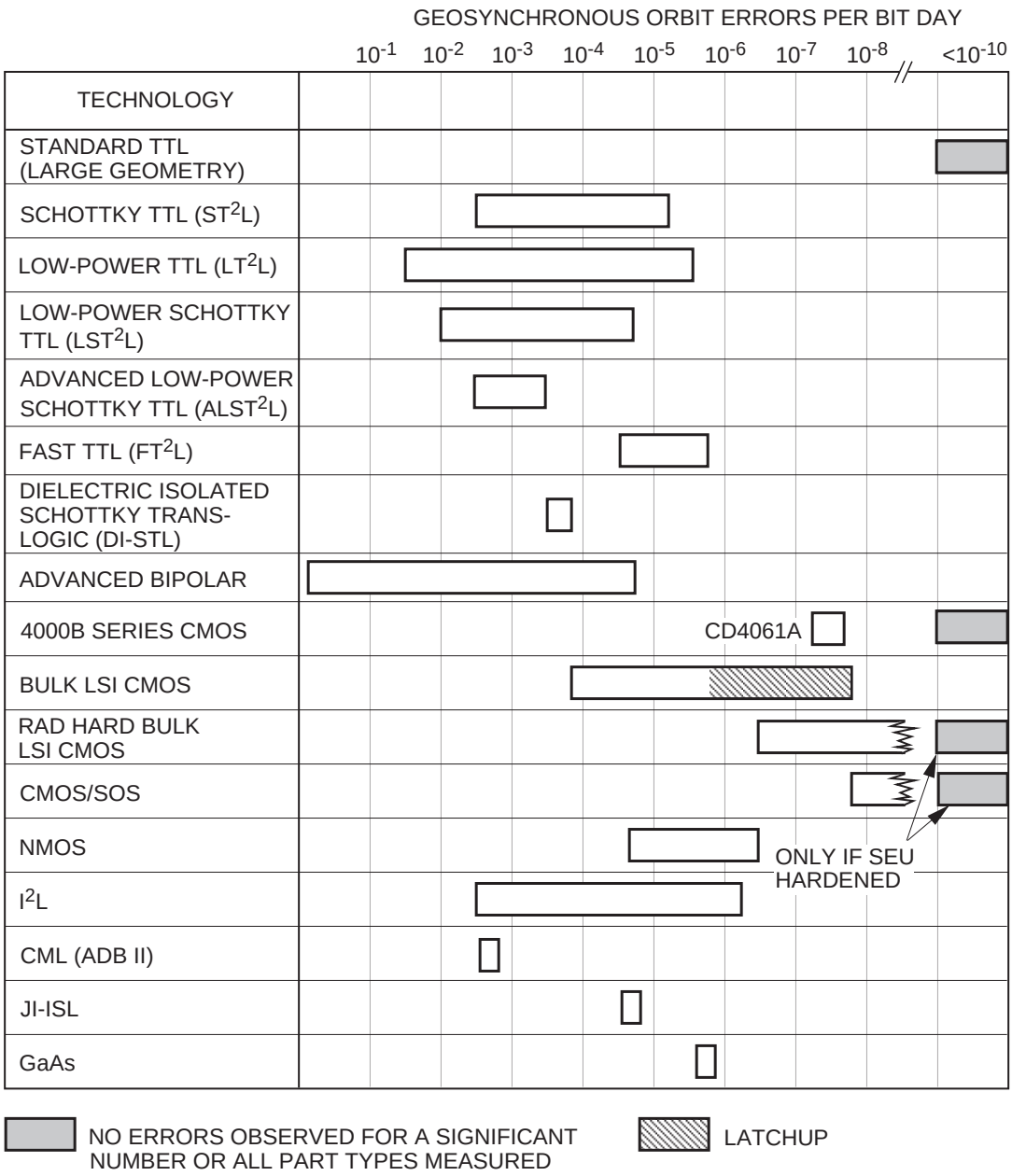

Figure 10-17. SEU rates at geosynchronous orbits for various circuit technologies. (From [13].)

In the case of TID effects, it is generally accepted that total-dose effects are not particularly dependent on the source of ionizing radiation. As long as the dose within the active regions of the circuit can be accurately measured and the characteristics of the radiation source are not significantly altered by the materials making up the part and its package, the absorbed dose in rads is a reliable measure of the extent of deposition of ionizing energy within the part. Thus, it is accepted practice to use Co^{60} radiation sources for total dose testing of devices and circuits. Co^{60} facilities have a variety of characteristics and vary in size from large rooms with thick concrete walls, as in the JPL Co^{60} facility, to small, self-contained irradiators that can be placed in standard laboratory settings. Co^{60} source rooms allow easy access and the ability to set up complex experiments, such as low temperature radiation exposures with parts under bias. Most

Co^{60} sources also provide for running cables outside the source so that parts can be biased and characterized *in situ* if necessary. With CMOS circuits, some form of part bias is nearly always necessary since, as we noted above, the part's radiation response will depend on bias and operating conditions during radiation exposure. Of particular importance are accurate and reproducible dosimetry techniques for establishing the dose received by the part. A standard method, MIL-STD 883, Method 1019.4, has been written for performing TID testing.

Transient high-dose-rate testing for the weapon-enhanced environment is much more difficult and challenging than TID testing. Dose rates in the range 10^9 rad(Si)/s to 10^{12} rad(Si)/s require large, specialized pulsed radiation machines, such as the HERMES pulsed X-ray machine at Sandia National Laboratory. Data acquisition schemes must be immune to machine-generated electrical noise and must cover a wide temporal range from nanoseconds to times as long as minutes in the case of extended part response, as for GaAs devices on semi-insulating substrates, optical fibers, and optoelectronic integrated circuits on insulators such as $LiNbO_3$. Dose-rate latchup testing is particularly difficult because latchup can exhibit unexpected behavior such as "latchup windows" [1], in which susceptibility to latchup disappears and reappears as the dose rate is increased. Also, in order to avoid consuming large numbers of parts in the testing sequence, some provision must be made for mitigating latchup before it destroys the test part. These difficulties have led to the development of less-expensive dose-rate simulation techniques, such as pulsed lasers that can be focused on specific areas of a part if needed. Often, however, it is necessary to expose large items such as circuit boards, and large pulsed machines are then a necessity.

To determine the effects of displacement damage on semiconductor devices and circuits, two types of radiation sources are generally used, depending on the particular radiation requirement to be satisfied. For the weapon-enhanced environment that has a neutron fluence requirement, radiation exposures are conducted with various neutron sources. Usually, the fluence requirement is large enough to necessitate a nuclear reactor as a neutron source. Reactors with undegraded fission neutron energy spectra are much better than reactors with some form of neutron moderation, such as water-moderated reactors, for several reasons: (1) the neutron energies are higher, which produces more efficient displacement damage; (2) there is much less radiation present of other types, such as energetic gamma rays and electrons; (3) the samples will not become nearly as radioactive because of the much lower thermal neutron fluences present; and (4) bare, fast-burst reactors such as those at Sandia and White Sands allow much easier experimental setup with large open spaces around the reactor core. A "clean" neutron source is particularly important when testing devices that are also susceptible to total-dose effects in order to avoid inadvertently degrading the circuit with ionizing energy deposition. Part characterization can be done either *in situ* or by testing the part before and after neutron exposure at the testing laboratory. Fortunately, in the case of neutron-induced displacement damage, room-temperature annealing is much less than in the case of TID damage in CMOS parts, so one can allow time for the disappearance of radioactivity and the transport of parts to different locations. In addition, displacement damage in the form of lattice displacements in the semiconductor bulk material is generally less dependent on whether or not bias is applied to the part during exposure. These features allow a "mail-order" method of conducting the testing in which parts are sent to a reactor facility, exposed in a container with no leads attached, and then returned later to the test laboratory for characterization.

Many applications in the natural space environment involve exposures to large fluences of energetic protons. For those parts that may be susceptible to displacement damage, such as Si and GaAs bipolar devices and circuits, solar cells, and LEDs, it is not

appropriate to substitute Co^{60} radiation exposure to satisfy a proton requirement. In parts that are sensitive to both ionizing radiation and displacement damage, such as Si BiCMOS circuits, it is customary to do both Co^{60} and proton testing in order to differentiate ionization effects from displacement damage effects. Proton-induced displacement damage effects tests are performed at accelerators that provide proton beams of various energies and fluxes. Compared with neutron-induced displacement damage, there are complications with proton testing that are associated with relating the accelerator test to actual space exposure. In the actual application, it is often difficult to predict the energy spectrum of the protons to which the part will be exposed because of the variation in solar proton spectra and the effects of spacecraft shielding on the energy spectrum. This situation is exacerbated by the fact that the amount of proton energy that is transferred to the semiconductor as displacement damage, often referred to as non-ionizing energy loss (NIEL), varies strongly with proton energy as the proton approaches the end of its track. If the proton comes to a stop in the active region of the device, large amounts of displacement damage will occur. On the other hand, test reproducibility and dosimetry are facilitated by using relatively high proton energies so that the proton's energy is not significantly degraded by the materials it must pass through to reach the device's active region. The net result of all this is that testing is often done between about 50 and 200 MeV at a few different energies, and then attempts are made to express proton fluences in damage equivalents at some standard proton energy such as 10 MeV.

Similar to proton testing, single event effects testing is also done away from the test laboratory at large, heavy ion accelerators such as those at Brookhaven National Laboratory, University of California at Berkeley, and Texas A&M. As in the case of neutron tests, proton displacement damage tests do not usually require *in situ* testing at the accelerator site, but SEE tests with both heavy ions and protons require part interrogation and characterization to be done during ion exposure (generation of "hard" or permanent errors in logic elements is an exception to this). Thus, SEE testing of sophisticated parts such as microprocessors is a particularly challenging activity. Test software and hardware development are complex, especially if one needs to independently determine the effects of upset in various sections of the part. Very often, one is attempting to test fast parts at speed, and this is complicated by long cables that run from the test equipment into the test chamber attached to the beam line, and by added electrical noise at the accelerator site. Complete part characterization requires the ability to change the angle of the beam to the part and to vary the temperature of the part. If the circuit is highly susceptible to total-dose damage, it will degrade after long-time beam exposure and may heat up in the test chamber vacuum because of total-dose-induced increases in leakage current. In addition, these machines usually run on a 24-h basis and cost on the order of $500/h to use. For SEU, it is desirable to obtain a complete LET versus cross section curve, which requires testing with different ions at a series of different angles. For latchup, on the other hand, it is often sufficient to determine a latchup threshold LET and a cross section at only one or two LET values. However, latchup testing must be done at the highest temperature expected in the application because SEL susceptibility increases with temperature. In both cases, it is also necessary to be able to vary the part bias during testing. All of these complicating factors have led to the development of other SEE simulation techniques. As in the case of dose-rate testing, pulsed lasers have proven useful but they are limited in their applicability and it is usually difficult to determine an absolute value of cross section. Another technique employs Cf^{252}, a naturally occurring fission source whose fission fragments have sufficient energy to cause single event effects. However, the energy of the fission fragments is not high enough to provide adequate penetration in many Si and GaAs parts. Thus, the Cf^{252} technique must be used as a pre-screen to be followed by accelerator testing if the part does not exhibit SEE during Cf^{252} exposure.

V. Radiation Effects in MMIC Devices and Circuits

In this section we review the work on radiation effects in MMIC devices and circuits in the same format as that used above for the background material on radiation effects in semiconductors. Radiation effects in microwave devices and circuits have been reviewed previously by others [10,20–22]. We will briefly summarize these earlier reviews and attempt to focus attention on more recent work. Although MMIC devices fabricated from Si (Si bipolar and Si/Ge heterostructure bipolar transistors (HBTs)) are in use, we will emphasize results for the III–V-based technologies. Before beginning this review, some general comments are in order with regard to the differences between Si and GaAs from the radiation effects point of view. Perhaps the most important difference is that GaAs devices and circuits do not contain SiO_2 oxide layers as gate insulators or as isolation insulators. In addition, the very high surface state densities typically found in the AlGaAs/GaAs system pin the Fermi level at the surface and effectively prevent radiation-induced surface inversion and its associated leakage currents from occurring. These differences result in GaAs devices being immune to total-dose effects until very high doses are reached where the rare displacement damage events caused by Compton electrons formed from Co^{60} gamma rays finally have an effect. Another important difference is the result of the fact that GaAs is a direct bandgap material in contrast with Si, which is an indirect bandgap semiconductor. This difference leads to the minority carrier lifetimes in GaAs being much less than those in Si. Thus, more displacement damage is required to affect GaAs devices that depend on minority carrier lifetime for their successful operation. The best example of this difference is the increased radiation hardness of GaAs solar cells relative to Si solar cells. With regard to device hardening techniques, the ability to perform "band gap engineering" in which layers of various materials can be grown on each other with little change in lattice constant, provides increased flexibility in the case of the III–V materials relative to Si. In spite of these positive features of the III–Vs, Si remains the material of choice for nearly all integrated circuits. Thus, its fabrication technology is very advanced and the cost of Si-based circuits is generally much less than similar circuits fabricated from III–V materials. This is the principal reason why GaAs digital circuits have never gained a great deal of popularity even though they have greater total-dose immunity.

A. Ionizing Radiation Effects

As noted above, GaAs devices in general, and MMIC GaAs circuits in particular, are relatively immune to total-dose effects resulting from the deposition of ionizing energy. This result is shown in Table 10-1, which provides tolerance levels for early Co^{60} radiation studies of MMIC devices. These results illustrate the natural hardness of GaAs MMIC devices to total-dose ionizing radiation. Again, this is due to the absence of an oxide that can trap charge and alter the operation of the device, and the fact that the gates of the GaAs transistors are controlled by junctions (JFETs) or metal Schottky barrier junctions (MESFETs). Other studies have also shown that GaAs MMIC devices are relatively insensitive to ionizing radiation total-dose effects [27–34]. An additional example of total-dose hardness levels near 100 Mrad(GaAs) is shown in Figure 10-18 for the saturation drain current in an enhancement mode GaAs JFET.

Table 10-1. Total-dose tolerance of various GaAs MMIC devices. (From [21]; courtesy of Artech House.)

Investigator	Element	Tolerance (rads(Si))
Newell, et al. [23]	MESFETs	2×10^8
Kodowaki, et al. [24]	MMICs	1×10^8
Aono, et al. [25]	Passive components	1×10^8
Morris [26]	MESFETs, IC	1×10^8

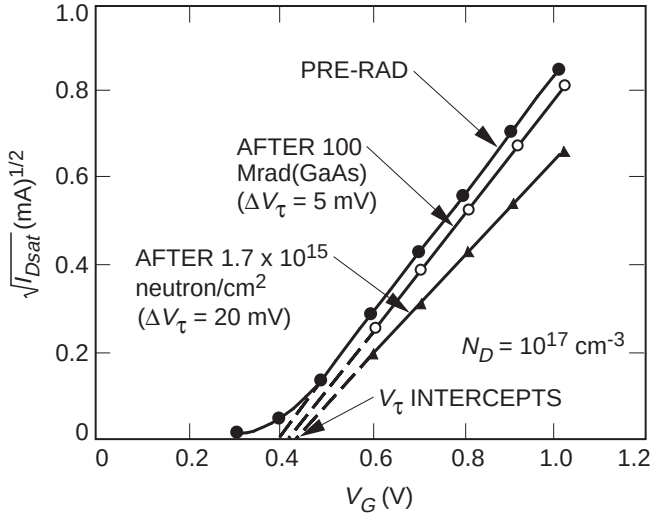

Figure 10-18. Change in saturation current of enhancement mode GaAs JFET after irradiation. (From [35]; ©1989 IEEE.)

A recent study [36] of the effects of gamma ray irradiation on a successive detection monolithic logarithmic amplifier (SDLA) hybrid consisting of both Si and GaAs chips also illustrates the difference in total-dose hardness between Si and GaAs devices. After irradiation to 8.7 krad, changes were observed in the dc bias point of the linearity output voltage, but the linearity shape was unchanged over frequency. These results led to the conclusion that the GaAs devices were unaffected by doses as large as 880 krad, but the Si Schottky diode in the temperature compensation circuit was susceptible to total-dose effects at low doses.

In contrast with the relative immunity of GaAs MMIC devices to total-dose effects, transient, high-dose-rate pulses can severely affect these devices. GaAs transistors and circuits have typically been fabricated on semi-insulating GaAs substrates, which afforded a natural isolation between individual transistors on the chip. However, in a transient radiation environment, this attractive feature becomes a liability because the transient photocurrents generated in the substrate are much larger than the transients generated elsewhere in the device [1,37]. During the ionization pulse, the large excess carrier densities that are generated in the semi-insulating substrate temporarily cause it to be a good conductor, allowing shunting of the transient photocurrent across transistor sources and drains. Under these conditions, upset levels in GaAs JFETs can be of the

order of 10^{10} rad(GaAs)/s (see Figures 10-11 and 10-12), or even less [37]. Fortunately, these effects can be minimized by properly placing bonding pads and metal interconnects, and by using various types of blocking layers.

In addition to large prompt photocurrents, long term transient effects have been observed in GaAs devices requiring several seconds to recover to normal behavior [1,10,21,22,35,38]. While prompt transients that last approximately as long as the ionization pulse can be dealt with by mitigation techniques, detrimental transient effects that last for many seconds are much more difficult to cope with because of long circuit down time. The long-term transient effect manifests itself as an observed reduction in drain current, often to very small values near zero, and a corresponding drop in output power, both of which recover slowly with time [22]. This effect, illustrated schematically in Figure 10-19, has been attributed to a back-gating mechanism due to strong trapping of radiation-generated carriers at mid-gap trapping levels in the substrate at the channel–substrate interface [39]. As indicated in Figure 10-19, the trapped charge induces a depletion layer that effectively pinches off the channel leading to a reduction in source-drain current. As the traps gradually empty following the pulse, the channel recovers and the drain current is restored.

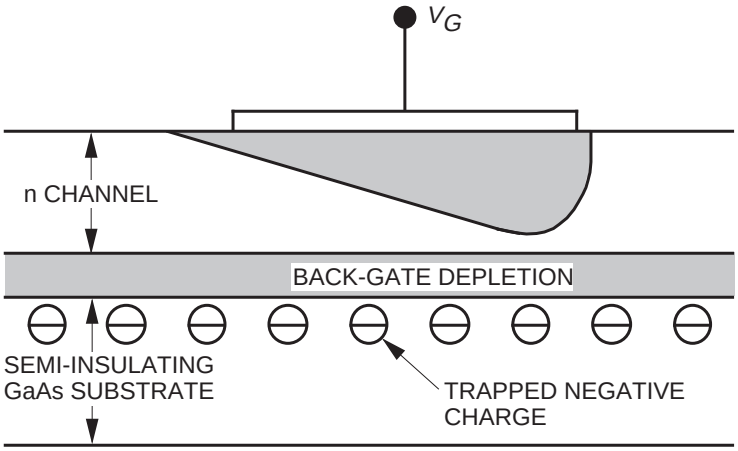

Figure 10-19. Cross section of GaAs JFET showing transient ionization-induced back-gating effect due to trapping of charge at mid-gap trapping levels near the substrate-channel interface. (From [39]; ©1986 IEEE.)

Several techniques have been developed to deal with the long-term transient problem in GaAs devices. Because semi-insulating GaAs contains large concentrations of compensating impurities, such as Cr, that introduce mid-gap traps, significant improvements can be obtained by using undoped substrates that are pure enough to provide fairly high resistivity. Comparative results using this technique are shown in Figure 10-20 for enhancement mode JFETs exposed to 20-ns wide pulses of 40-MeV LINAC electrons [40]. Note that the drain current in the JFET on the undoped substrate essentially follows the pulse, but the JFET on the Cr-doped semi-insulating substrate exhibits a long-lasting tail in the drain current recovery. In another technique used to eliminate substrate back gating, a buried p-layer is implanted below the active n-channel to act as a blocking layer for trapped carrier effects in the substrate [41]. The dramatic improvement that can be obtained with this method is shown in Figure 10-21 for GaAs JFETs fabricated on the same chip. In the case where there was a Be-implanted layer below the Si-implanted active region, only the response to the pulse was seen, but in the Si-implanted device with no buried p-layer, there is a long-term drain current transient due to back gating. We noted earlier that the ability to do bandgap engineering in which

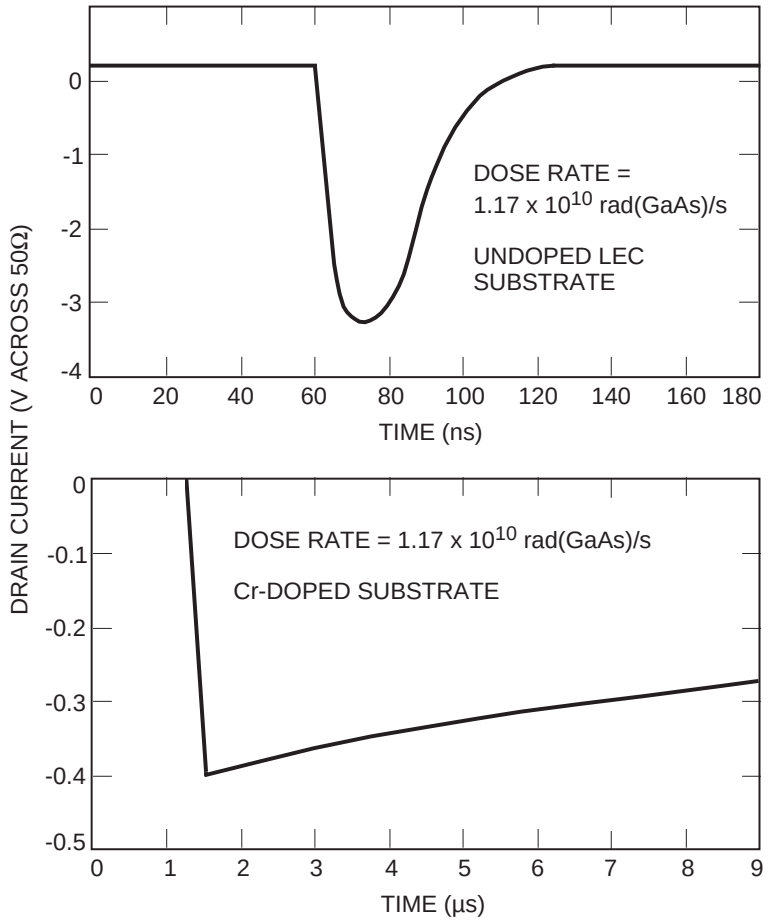

Figure 10-20. Transient response of drain current to 20-ns electron pulses for GaAs JFETs on two types of substrates (V_{GS} = 0 V, V_{DS} = 5 V). (After [40]; ©1982 IEE].)

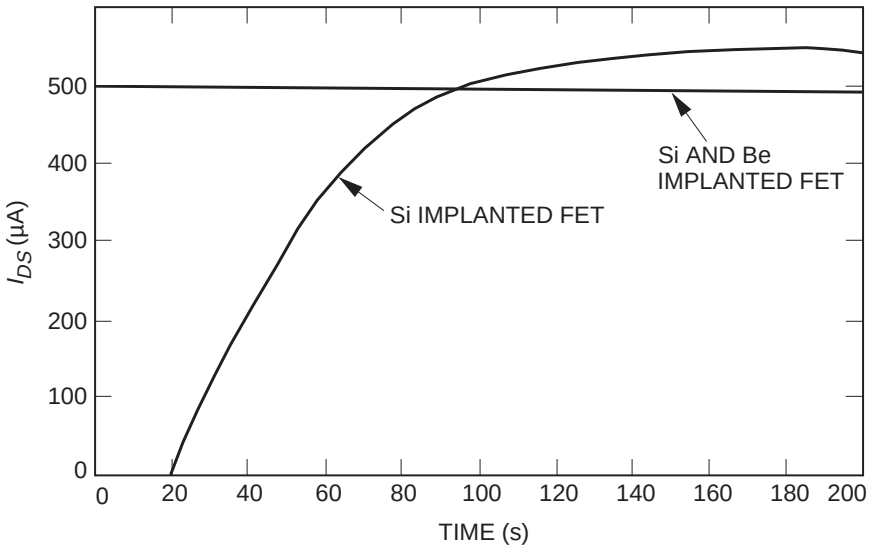

Figure 10-21. Transient drain current response for single- and double-implanted GaAs JFETs. (From [41]; ©1982 IEEE.)

one grows layers of various types, can facilitate hardening of a III–V device to radiation effects. Another technique for minimizing back gating is based on adding an AlGaAs buffer layer below the active GaAs channel regions of the FETs on the chip [39]. Using molecular beam epitaxy (MBE), an AlGaAs buffer layer was grown to block substrate back-gating effects from both depletion and enhancement mode GaAs FETs. The transient response of these devices to 50-ns electron pulses was a factor of 100 less than that of similar devices without the AlGaAs buffer layer.

In addition to the GaAs transistors discussed above, a variety of MMIC devices have also been subjected to transient, high-dose-rate testing. For example, a Texas Instruments two-state feedback amplifier MMIC, fabricated by Si implantation into semi-insulating substrates, was exposed to 50-ns-wide, 40-MeV electron pulses while operating under normal bias at X-band frequency [22,34]. Upsets in the power output that lasted approximately 4 μs over a dose-rate range of about $1x10^8$ rad(GaAs)/s to $2x10^{11}$ rad(GaAs)/s were observed. The growth in the peak-to-peak magnitude of these output power upsets as a function of increasing dose and dose rate is shown in Figure 10-22. At a dose rate approaching $2x10^{11}$ rad(GaAs)/s, the peak-to-peak upset in the output power is approximately equal to the absolute value of the operating output power. Additional studies [42,43] of TI MMIC feedback amplifiers led to the following conclusions regarding hardening of MMICs to transient upset: (1) minimize metal lines in direct contact with substrate, (2) minimize off-chip bypass capacitors, (3) use resistors to limit capacitor discharge during pulse exposure, and (4) use series inductance to reduce drain-source voltage during radiation pulse. These results suggest that a combination of prudent MMIC circuit design and the use of blocking layers will significantly reduce the sensitivity of MMICs to transient effects.

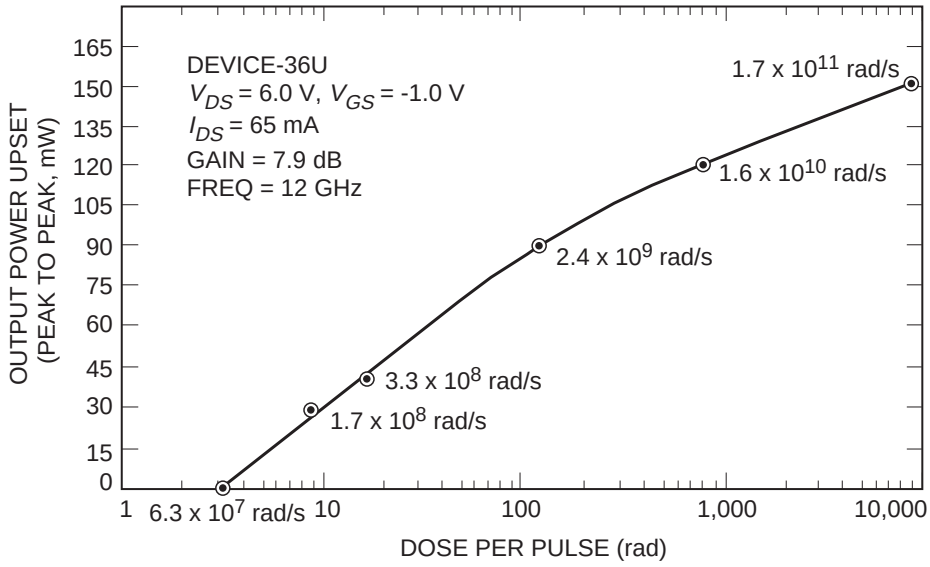

Figure 10-22. Peak-to-peak power upset generated by 50-ns pulses of 40-MeV electrons bombarding TI two-state feedback amplifier MMICs. (From [34]; ©1985 IEEE.)

In a combined total-dose and transient upset study [31], the radiation response of two types of MMICs was examined: (1) a broadband distributed amplifier fabricated by ion implantation into a semi-insulating substrate, and (2) a Ka-band power amplifier

employing epitaxially grown buffer and active layers on a semi-insulating substrate. Shown in Figure 10-23 is the temporal response of output power to a 50-ns-wide pulse of 40-MeV electrons at a dose rate of approximately 2×10^{11} rad(GaAs)/s for both types of MMICs. Note that the power output of the broadband amplifier is zero for several microseconds, but that the output of the Ka-band amplifier never falls to zero, and actually recovers within 3 μs. While circuit design differences can account for some of the variations in radiation response, it is tempting to conclude that the greater immunity of the Ka-band amplifier is due to the use of epitaxial active and buffer layers. The fact that this amplifier puts out power through a very large dose-rate pulse is encouraging for application of these MMICs in military environments. Additional combined radiation environment (flash X-ray and pulsed neutron) studies have been performed more recently on GaAs MMICs fabricated at Texas Instruments by implantation into low Cr-doped LEC substrates [44,45]. Bearing in mind that the Cr is responsible for deep traps in the substrate material and that there were no blocking layers, it is not surprising that flash X-ray exposures at levels near $1x10^{11}$ rad(GaAs)/s caused long-term transients in the drain current in these distributed amplifiers.

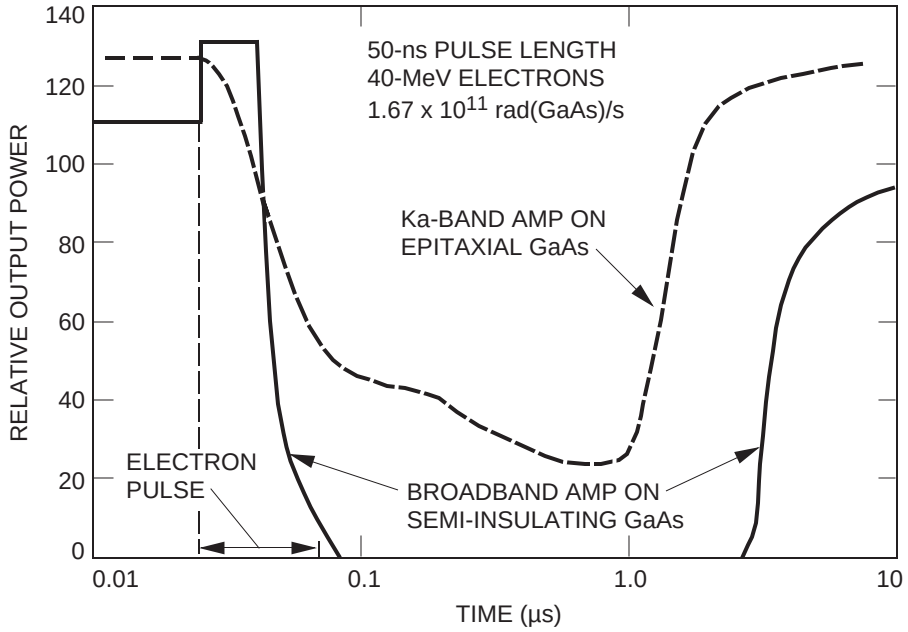

Figure 10-23. Response of MMIC amplifiers to transient electron pulses. (After [31]; © 1988 IEEE.)

B. Displacement Damage Effects

As indicated in Figures 10-13 and 10-14, and as pointed out earlier, GaAs devices are relatively insensitive to displacement damage effects when compared to Si devices. Generally, this is due to the shorter minority carrier lifetimes and higher doping levels found in GaAs devices and circuits. Since the displacement damage introduced into the semiconductor material reduces the minority carrier lifetime, the mobility, and the carrier concentration, device properties that depend on these parameters will be affected by displacement damage. Generally, the longer the lifetime, the higher the mobility, and the smaller the carrier concentration the more effective displacement damage is in altering these parameters. Thus, semiconductor devices with short lifetimes, low mobilities, and high carrier concentrations will be relatively immune to displacement damage effects.

Unfortunately, devices with these properties do not necessarily produce the highest performing circuits. In particular, microwave circuits must be very fast since they operate at high frequencies. Thus, lifetimes should be short and mobilities should be high, characteristics generally true of GaAs devices. Therefore, we can expect that GaAs MMICs will be sensitive to displacement damage through a reduction in mobility, and also carrier concentration if the active device regions are lightly doped.

Although the carrier removal rate due to displacement damage in n-type Si is roughly half that of the carrier removal rate in n-type GaAs (partially due to anneal of some of the damage in Si), the displacement damage-induced changes in JFETs made from either material are about the same. This is shown in Figure 10-24 in which the neutron fluence necessary to reduce the JFET transconductance, g_m, by 20% is plotted vs the initial carrier concentration [46]. Note also that, as one would expect, the higher the pre-irradiation carrier concentration, the less sensitive the JFET is to irradiation. In fact, if the doping level is high enough, these JFETs are essentially immune to typical military neutron fluence requirements. In the case of the natural space environment, displacement damage will be due to exposure to protons that are more effective at creating displacement damage than neutrons on a per unit fluence basis. If one assumes that protons are 50 times more effective, a factor typical of both Si and GaAs, examination of Figure 10-24 indicates that these JFETs will be essentially immune to typical proton requirements for NASA and commercial space applications. This conclusion is based on the observation that the lower ends of the curves in Figure 10-24 are at about 5×10^{13} neutrons/cm^2, which is roughly equivalent to 1×10^{12} protons/cm^2, and this proton fluence is equivalent to a dose in excess of 200 krad for 50 MeV protons.

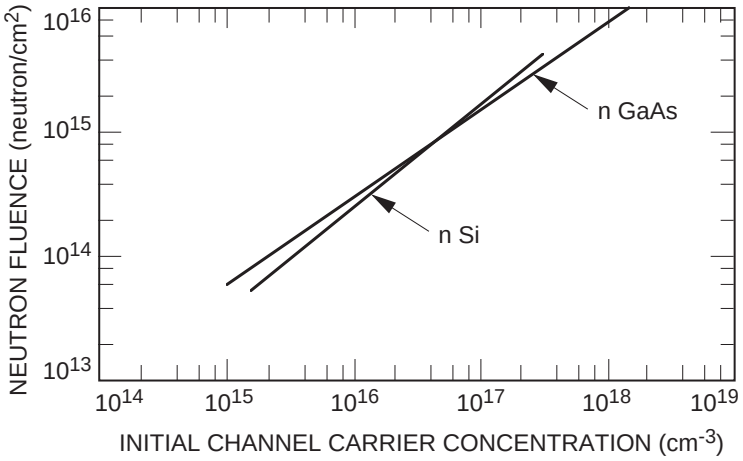

Figure 10-24. Neutron fluence necessary to reduce JFET transconductance by 20% in n-type GaAs and Si. (From [46]; ©1967 IEEE.)

Relative to other types of transistors, microwave devices have greater radiation hardness because of their high operating frequency, which requires short minority carrier lifetimes and reduced base widths. This is illustrated in Figure 10-25 for gain degradation of a variety of transistor types [47]. Note that high-power devices with their large feature sizes and thick base regions are most sensitive, and that microwave transistors are least vulnerable, and do not show gain degradation until fluences above 10^{13} neutrons/cm^2 are reached.

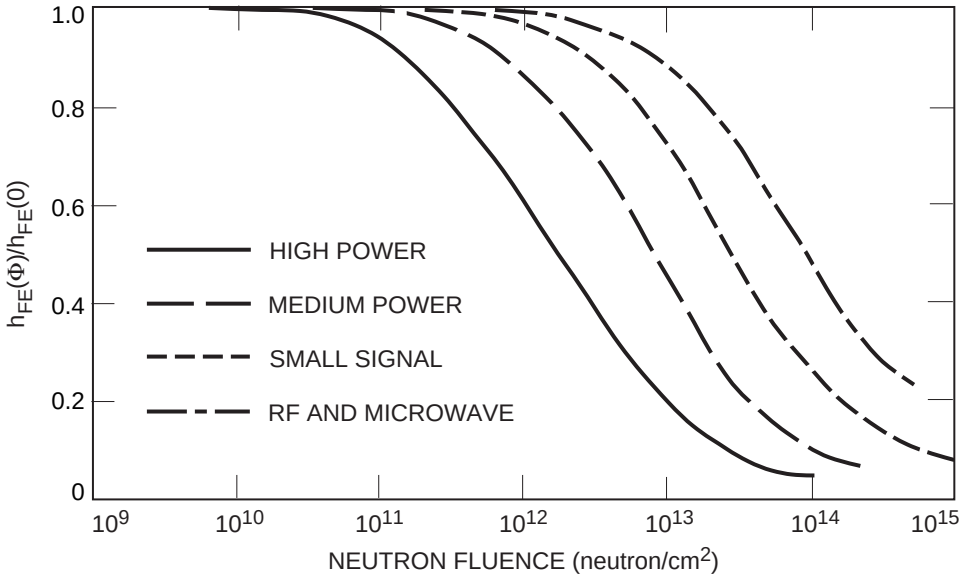

Figure 10-25. Gain degradation of several types of bipolar transistors. (From [47]; ©1984 IEEE.)

Additional neutron irradiation data illustrating the hardness of GaAs FETs to displacement damage is shown in Figure 10-26 for transistors fabricated at Texas Instruments by implantation into semi-insulating substrates [22,34]. Note that the small signal gain does not decrease significantly until fluences near 10^{15} neutrons/cm^2 are reached. The transconductance was similarly insensitive to neutron irradiation. The drain current began to decrease at lower neutron fluences, but the hardness level was still satisfactory for nearly all conceivable applications. The most sensitive parameter was pinch off voltage (not shown in Figure 10-26), which started to decrease due to carrier removal at fluences as low as 4×10^{13} neutrons/cm^2.

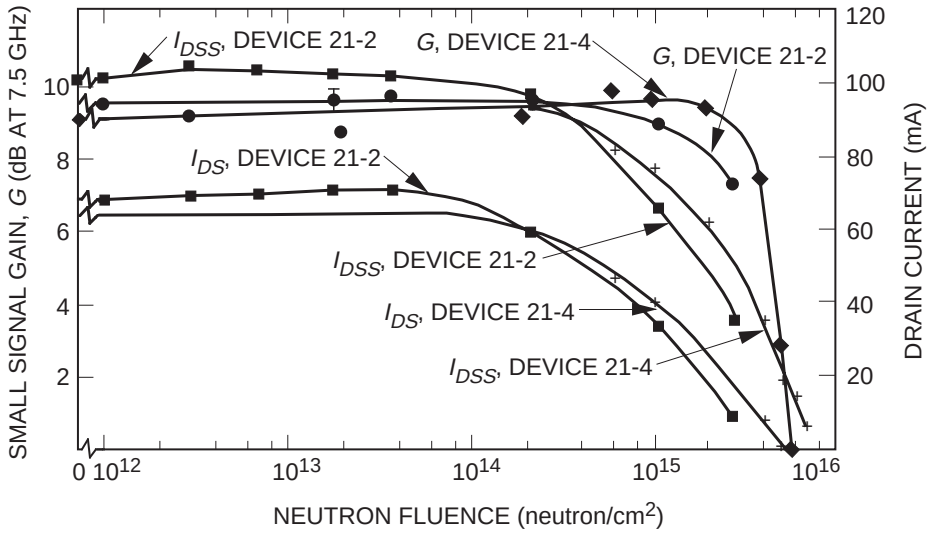

Figure 10-26. Effect of neutron irradiation on TI GaAs FET parameters. (From [34]; ©1985 IEEE.)

Additional examples of the relative immunity of GaAs FETs and MMICs to displacement damage have been given in other studies. In Figure 10-18 in addition to the total-dose results, the decrease in drain current due to an irradiation of 1.7×10^{15} neutrons/cm^2 is shown [35]. Note that for an n-channel donor doping level of 1×10^{17} cm^{-3}, there is not a large change in drain current as a function of gate bias, even for this large fluence irradiation. Neutron-induced effects have also been examined in the same two types of MMICs as shown in Figure 10-23 [30] for pulsed electron bombardments. In that case, the device fabricated on epitaxial material was less susceptible to radiation effects, and as suggested by the results in Figure 10-27, the same is true following neutron irradiation. Following irradiation, rebiasing of the broadband amplifier to recover the gain was only partially successful, while in the case of the Ka-band amplifier on epitaxial GaAs, the gain was restored by rebiasing. In addition, the frequency response of the Ka-band MMIC actually improved after irradiation.

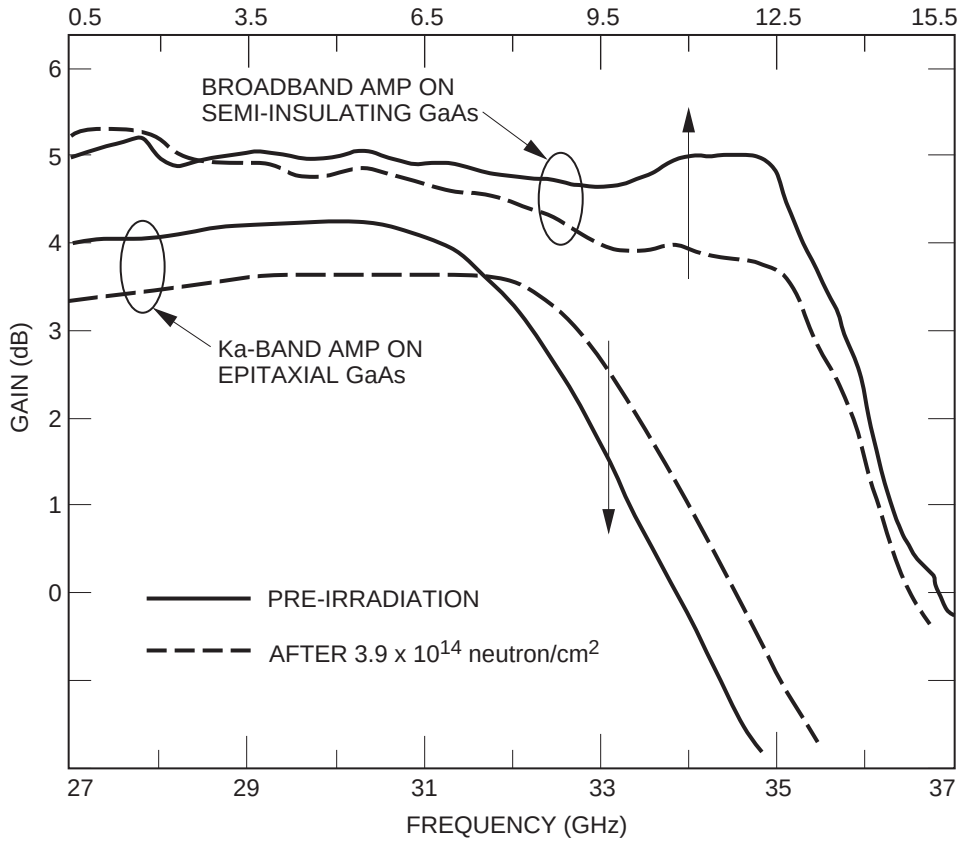

Figure 10-27. Response of two GaAs MMIC amplifiers to neutron irradiation. (After [30].)

In two studies [44,45] mentioned earlier in our discussion of prompt dose-rate upset, pulsed neutron irradiations were done on GaAs FETs and MMICs in conjunction with flash X-ray exposures. In addition to the X-ray-induced long-term drain current transients noted earlier, neutron pulse exposure also produced drain current transients. In addition, it was noted that some of the neutron induced damage appeared to anneal out following the neutron pulse. To some degree, the transient effects of flash X-ray bombardment and simultaneous pulsed neutron exposure served to cancel each other out, so that the combined effects were not as severe as either irradiation by itself. However, this must be viewed as a fortuitous occurrence that cannot be generalized to other

conditions and devices. It is also important to note that the neutron pulses were accompanied by pulses of gamma rays, which also contribute to the overall transient effects. This work was extended [45] to include the effects of varying the temperature on the resultant transients following flash X-ray and pulsed neutron bombardment. As one might expect for an effect dominated by substrate trapping behavior, the drain current transients were extended to longer times as the temperature was lowered.

Proton bombardment studies of GaAs MMICs have been relatively rare, but as we noted above, one can at least infer the effects of proton-induced displacement damage from neutron irradiation studies. In one recent study [48], the authors examined displacement damage effects in GaAs FETs, MMICs and HEMTs (high electron mobility transistors) due to bombardment with 14.5 MeV Si ions, 15.7 MeV O ions, 1 to 3 MeV alpha particles, and 2 MeV protons. The results of this study are summarized in Table 10-2, which shows the particle fluence necessary to degrade the drain current by 20%. Generally, the HEMTs are less sensitive to irradiation than the other device types. This is because drain current degradation occurs by carrier removal in the heavily doped AlGaAs layer in the HEMT rather than in the 2DEG (2 dimensional electron gas) channel. In addition, while displacement damage due to these ions causes mobility reductions, the scattering dynamics of the 2DEG are different, resulting in somewhat greater immunity to displacement damage. Notice that the MMIC device showed significant degradation after 6×10^{11} 2-MeV protons/cm^2. Recalling that we pointed out in our discussion of Figure 10-24 that proton-induced degradation would not be significant until at least a fluence of 1×10^{12} protons/cm^2 was reached, this result in Table 10-2 suggests greater sensitivity to proton irradiation. Note, however, that we have also emphasized that displacement damage is greatest near the end of a particle's track, and that these protons are low energy (2 MeV). Considering that the 2-MeV protons had to pass through overlayers before reaching the active regions of these devices, it is not surprising that the devices are sensitive at somewhat lower fluences. We emphasize, however, that fluences above 5×10^{11} protons/cm^2 are still fairly large for typical NASA and commercial space applications, and the protons encountered in the space environment will be of much higher energy.

Table 10-2. Ion-bombardment-induced degradation of drain current in GaAs devices. (From [48]; ©1990 IEEE.)

Ion	Ion Energy (MeV)	Device	Fluence at 20% Degradation in I_D (cm^{-2})
H	2.0	HEMT-V3	2.3×10^{12}
	2.0	HEMT-V7	3.0×10^{12}
	2.0	MMIC	6.2×10^{11}
He^4	1.1	FET	1.5×10^{9}
	3.0	HEMT-V7	3.0×10^{11}
	3.0	MMIC	6.6×10^{9}
O^{16}	15.7	MMIC	1.0×10^{9}
Si^{28}	14.5	HEMT-V3	5.2×10^{9}
		MMIC	4.1×10^{9}
		HEMT LNA-C	4.2×10^{9}
		FATFET	2.5×10^{9}
		HEMT-C	1.8×10^{9}
		FET-C	7.4×10^{9}

C. Single Event Effects

Most of the recent studies [18,49–62] of single event effects in GaAs devices have focused on charge collection mechanisms in individual transistors of various types. The intent of much of this work has been to discover and define charge collection in GaAs devices so that GaAs SRAMs can be hardened to SEU effects. However, it is not clear that GaAs memories will ever be used to any significant extent in space environments. In any case, these basic studies of charge collection also provide information that is beneficial to MMIC development, although additional SEE investigations on MMICs themselves need to be accomplished.

Studies of charge collection in GaAs devices have shown that charge generated by a single particle can be collected by a greater variety of mechanisms than in Si devices. The diagram in Figure 10-28 illustrates some of the possible charge collection paths following an ion strike in a GaAs MESFET [63]. Collection from deep within the device is limited because the recombination rate in GaAs is high, and because the diffusion length is short due to small minority carrier lifetimes. However, relative to Si, this is offset by the fact that more regions of the device are sensitive than in the case of a Si MOSFET. In the GaAs MESFET shown in Figure 10-28, the source and drain regions are sensitive to upset as well as the gate region. Collection mechanisms for the various regions in the device have been studied, and these include a back channel turn-on mechanism [53,57–59], a bipolar source-drain collection mechanism [51,55,56,58,60,61], and an ion shunt mechanism [50,52,54]. As shown in Figure 10-28, following the ion strike, electrons will be collected at the drain, and holes will be collected at the gate under

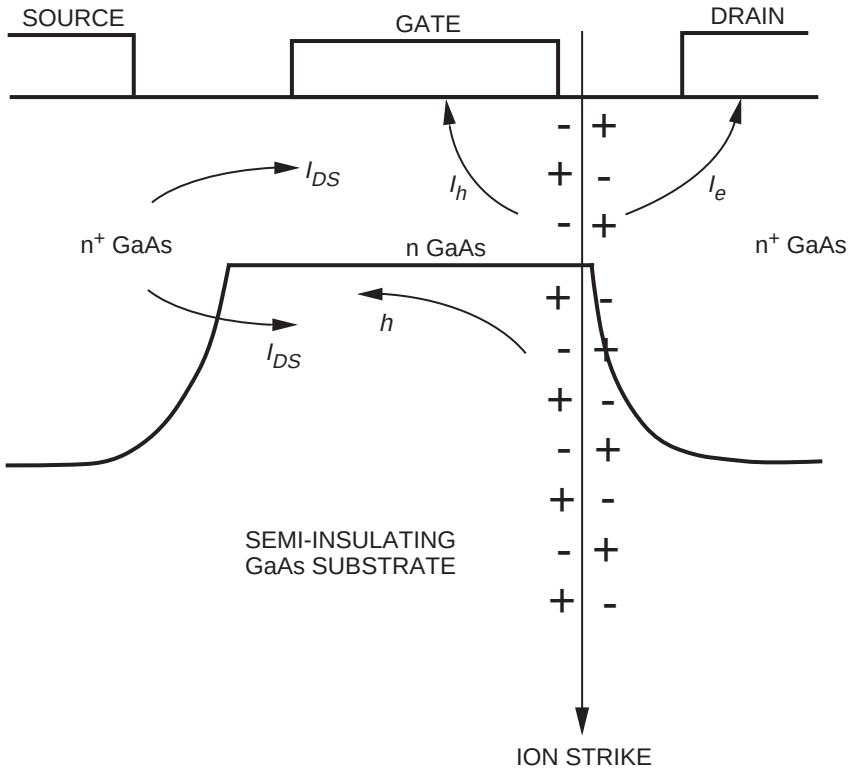

Figure 10-28. Single-particle-induced charge collection mechanisms in a GaAs MESFET. (From [63]; ©1994 IEEE.)

normal bias conditions for a MESFET. Alterations in the electric field caused by the ion will result in the lowering of the source potential barrier as holes flow toward the source, and the MESFET will partially turn on, leading to increased electron flow from source to drain and a transient drain current. A significant portion of this current will flow in the substrate as long as there is an electron concentration present that is comparable to the built-in space charge at the channel-substrate interface. Thus, collection times for the source-drain mechanism can be hundreds of picoseconds, much longer than that for the standard collection mechanism. The total charge collected at the drain in this manner can significantly exceed that collected at the gate by the usual SEU charge mechanism. In complex structures involving several heterolayers, the ion shunt mechanism can result in charge flow between layers and individual transistors due to the transient conduction caused by the ion in normally blocking or insulating regions. This mechanism can also operate in a Si circuit laterally between transistors when feature sizes are small and a highly penetrating (energetic) ion strikes the circuit surface at an oblique angle.

The above discussion suggests that there is no single, simple conclusion one can reach concerning the susceptibility of GaAs circuits to SEU, relative to that of more traditional Si circuits. However, merely on the basis of the relatively larger currents prevalent in bipolar GaAs MMICs, one can argue that these circuits will demonstrate a greater hardness to SEE than GaAs or Si digital devices. It does not follow, however, that there is no need to examine SEE effects in MMIC circuits, especially as this technology evolves into more sophisticated and widely used devices. In perhaps the only study to date specifically devoted to SEE in MMIC devices, Barillot, et al [64] examined the sensitivity to single event burnout (SEB) of four types of commercial microwave devices, the characteristics of which are shown in Table 10-3.

Table 10-3. Characteristics of four GaAs microwave transistors examined for SEB. (From [64]; ©1996 IEEE.)

Characteristics	Device (Manufacturer)			
	MESFET HAV (Triquint)	MESFET F20 (GEC-Marconi)	Heterojunction HFET (Texas Instruments)	PHEMT MMC046A (Raytheon Electronics)
Process	Implant	Implant	Epitaxy	Epitaxy
Recess	Single	Single	Double	Double
Gate metal	Au/Pd/Ti	Au/Pd/Ti	Au/Pd/Ti	Au/Pd/Ti
Total gate width (μm)	300 (6×50 μm)	300 (4×75 μm)	600 (10×60 μm)	100 (1×100 μm)
Drain-source distance (μm) (measured)	4	5.6	3.9	2.6
Gate length (μm)	0.5	0.5	0.5	0.25
V_{gd} (V) max rating	7.5	8	16	11
V_{ds} (V) max rating	7.5	6	13.75	10.5

Iodine ions were used at various angles (maximum effective LET of 71.8 MeV-cm^2/mg) to test these four transistor types for SEB as a function of applied bias. No ion-induced burnouts were observed at the maximum rated bias voltages given in Table 10-3. Burnout was observed in all four transistors, but only at voltages above the rated maximum bias levels (V_{gd} values for burnout: 10 V for Triquint, 9 V for GEC-Marconi,

20 V for TI, and 19 V for Raytheon). Thus, these devices are not susceptible to SEB under normal operating conditions.

VI. Conclusions

In this review we have summarized the current understanding of the effects of radiation on GaAs monolithic microwave integrated circuits (MMICs) and devices. With one important exception (transient, high-dose-rate effects), one can broadly state that these devices are significantly more immune to radiation effects than traditional Si digital and bipolar technologies. MMICs are essentially immune to total-dose effects, and are susceptible to displacement damage only at relatively large neutron and proton fluences, especially if active device regions are relatively heavily doped as is often the case. Single event effects can be problematic because of source–drain currents induced in semi-insulating substrates, but general SEE susceptibility is relatively low, although more work needs to be done in this area.

One must draw a distinction between military and civilian space applications because of the presence of large transient dose-rate pulses in the nuclear-weapon-enhanced space environment. We have seen that MMIC devices fabricated directly in semi-insulating substrates are susceptible to large transient effects that can last for several decades in time beyond the termination of the radiation pulse. These effects are not an issue for a typical NASA natural space environment mission.

It is interesting to contrast the potential availability of hardened GaAs MMICs with that of traditional Si digital circuits and devices. In the Si world, availability of devices is driven strongly by the commercial market, and space applications do not represent enough of a market to allow hardening modifications of marketable circuits. Thus for Si digital space electronics, one is restricted to using a very few suppliers, to hardening by circuit design if it does not impact commercial production, and to the use of circumvention and mitigation techniques, such as shielding, with commercially available products.

The commercial marketplace for GaAs MMICs is much smaller than that for Si digital and bipolar circuits, and can be viewed as much more of a custom-device-oriented activity. Thus, the framework in which one must alter part design and fabrication to achieve radiation hardness is much more receptive to these customized designs, and it is possible to acquire custom products from “commercial” suppliers. This is fortunate, since there are fairly obvious changes that can be made to harden GaAs MMICs. Probably the most important is to avoid building parts in semi-insulating GaAs, or at the very least, using semi-insulating material only as a substrate for growing layers by a technique like MBE or MOCVD so that bandgap engineering can be used to isolate the substrate from active device regions. In this way, one can mitigate long-term high-dose-rate-induced transient effects and large single-event-induced source–drain currents. For those applications where either the neutron or proton fluence requirement is large, one can heavily dope active regions so that carrier removal is less, or use HEMTs to achieve high mobility in conjunction with heavy doping to achieve hardness without sacrificing performance.

Although GaAs MMICs are relatively immune to radiation effects, as the technology evolves, radiation-effect studies and testing will still be necessary to insure that technology advances do not result in increased vulnerability to radiation. Certainly, for Si-device technologies, this has been a perennial problem. Of particular interest in the future will be technologies that combine various materials—such as Si, GaAs, and optical

materials—on single substrates to achieve maximum microwave, optical, and digital processing performance. These future “instruments on a chip” will require extensive reliability and radiation studies to insure their potentially powerful performance in the space environment.

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