DEPARTMENT OF INFORMATION ENGINEERING

UNIVERSITY OF PADOVA

Ionizing Radiation Effects on Advanced CMOS Technologies

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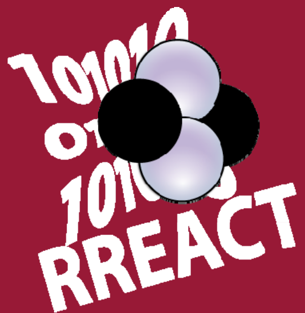


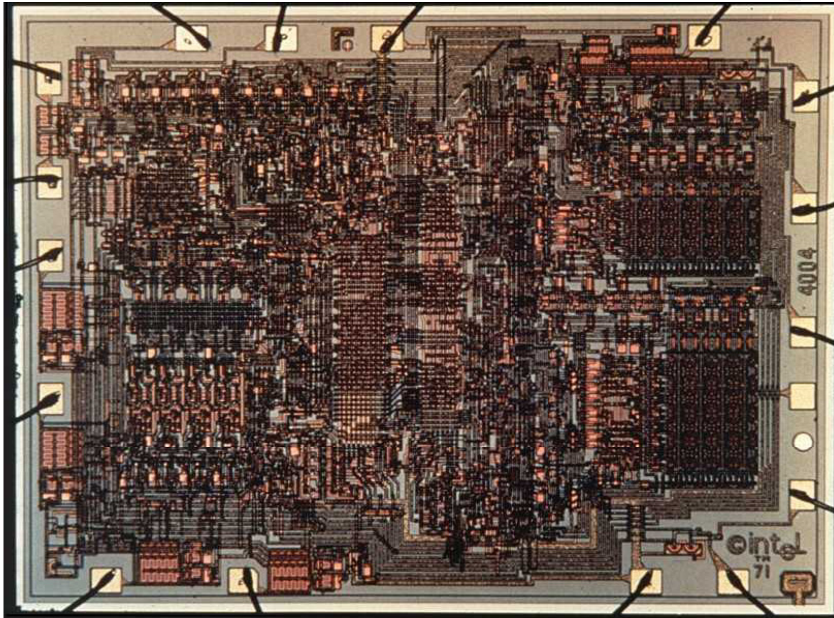
Reliability and Radiation Effects on Advanced CMOS Technologies

Theme

- What is the impact of **CMOS technology evolution** on the **radiation sensitivity** of modern digital integrated circuits?
- As we explore this issue, we will investigate in more details the **basic mechanisms** underlying the radiation response of CMOS circuits

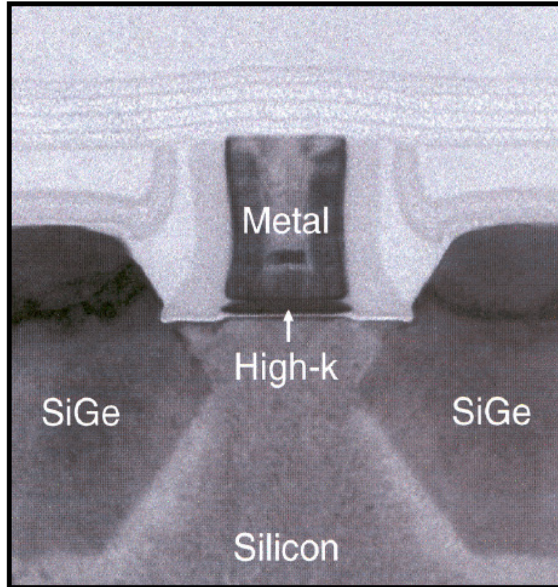
- CMOS Scaling
  - Feature Size
  - New Materials and Architectures
  - Frequency
- Total Ionizing Dose
  - Basic Mechanisms
  - Impact of Scaling
  - New Phenomena
- Single Event Effects
  - Single Event Upsets
  - Single Event Transients

- How to make it faster?
- Until early 2000's
  - **Scaling**!
- Afterwards
  - Scaling and…
  - New **materials**
  - New device **architectures**



Intel 4004 featuring 10-μm MOSFETs

www.intel.com/museum



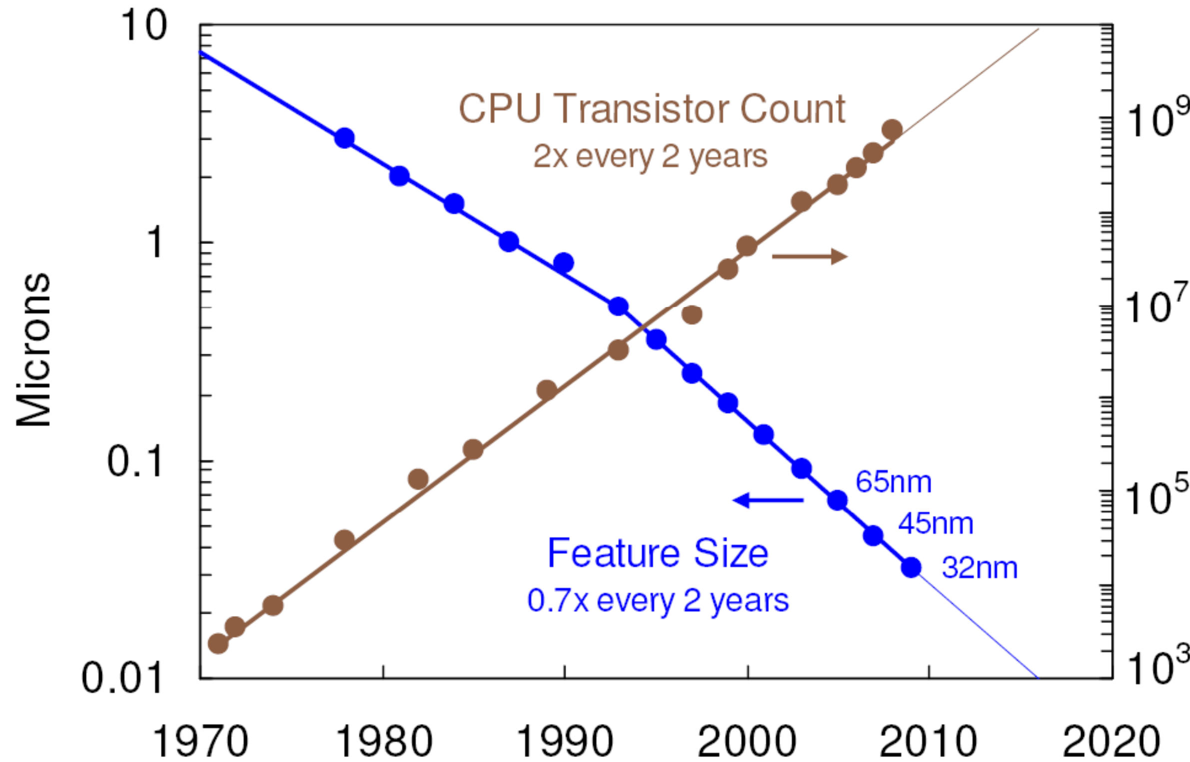
Core 2 Duo transistor
Intel 45-nm node, featuring strained silicon, high-k gate oxide, and metal gate

M. Bohr, ISSCC 2009

- How to make it faster?
- Until early 2000's
  - **Scaling**!
- Afterwards
  - Scaling and…
  - New **materials**
  - New device **architectures**

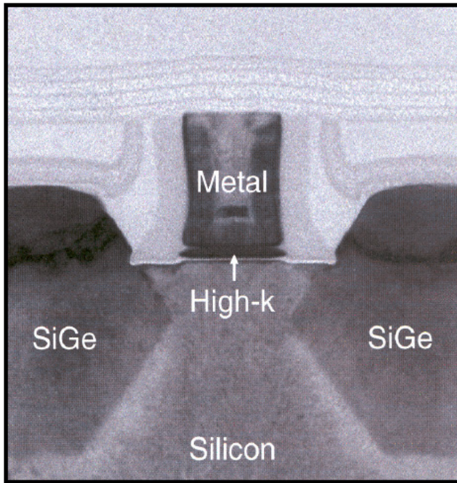
Parameter	Scaling Factor
Feature Size t_{ox}, L, W	1/k
Doping	k
Voltage	1/k
Current	1/k
Capacitance	1/k
Delay Time	1/k
Power Dissipation	$1/k^2$
Power Density	1

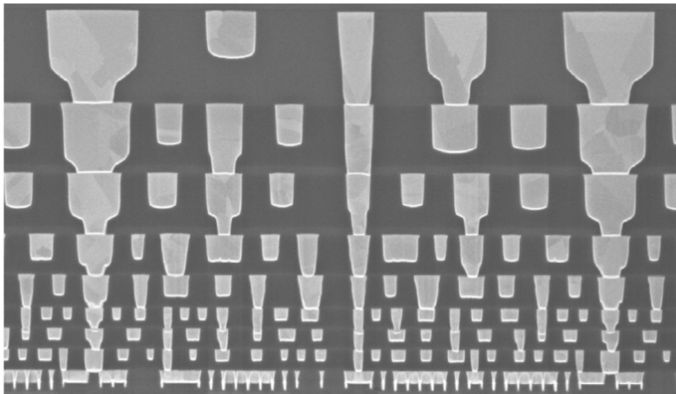
- Scaling of operating voltage has actually been slower than feature size reduction



M. Bohr, ISSCC 2009

- Exponential decrease of the feature size with time
- Exponential increase in transistor count

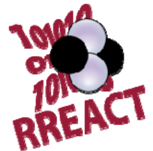




www.intel.com/research

- **Transistors**
  - High-k gate oxide ⇒
    - ↑ channel control
    - ↓ leakage
  - Strained Silicon ⇒
    - ↑ drive current
  - Silicides
    - ↓ series resistance
- **Back-end**
  - Low-k inter-metal layers
    - ↓ stray capacitance
  - Copper vs Aluminum
    - ↓ series resistance

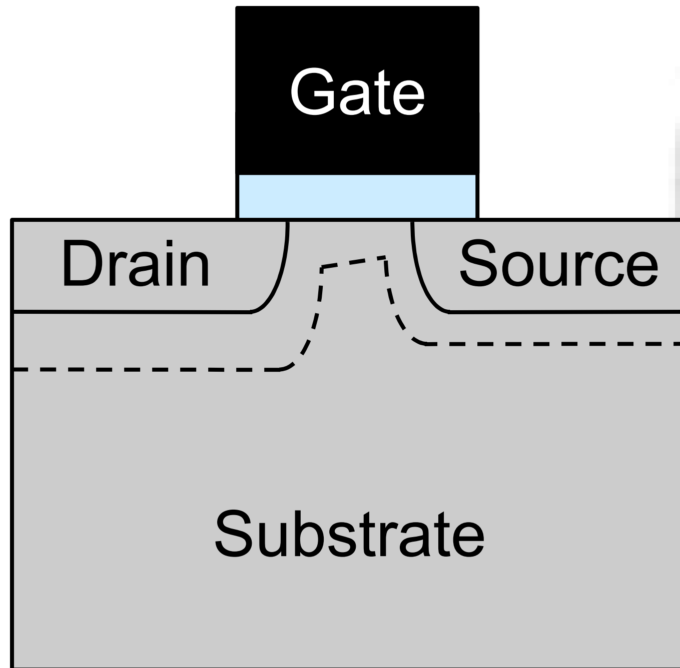
H																	He
Li	Be											**B**	C	N	**O**	F	Ne
Na	Mg											**Al**	**Si**	**P**	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	**As**	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac	Rf	Db	Sg	Bh	Hs	Mt	Ds								
		Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu		
		Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr		



H																	He
Li	Be											**B**	C	N	**O**	F	Ne
Na	Mg											**Al**	**Si**	**P**	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	**As**	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac	Rf	Db	Sg	Bh	Hs	Mt	Ds								
		Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu		
		Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr		

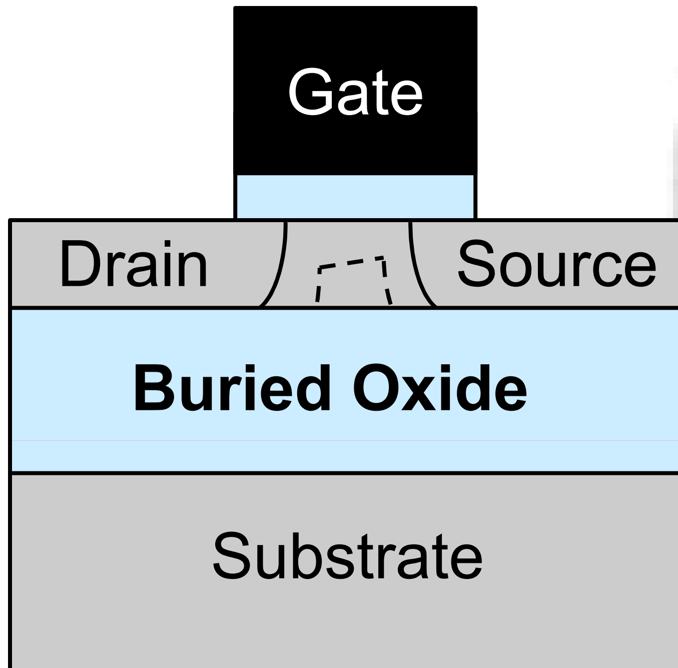
CMOS Materials today

H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac	Rf	Db	Sg	Bh	Hs	Mt	Ds								
		Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu		
		Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr		



Bulk MOSFET

- Silicon On Insulator (SOI)
  - Partially Depleted
  - Fully Depleted
  - Double Gate
  - FinFETs
- Several Advantages
  - Reduced Capacitance
  - Improved Electrostatics $\Rightarrow$ Better Short Channel Effects



Partially Depleted SOI MOSFET

- Silicon On Insulator (SOI)
  - Partially Depleted
  - Fully Depleted
  - Double Gate
  - FinFETs
- Several Advantages
  - Reduced Capacitance
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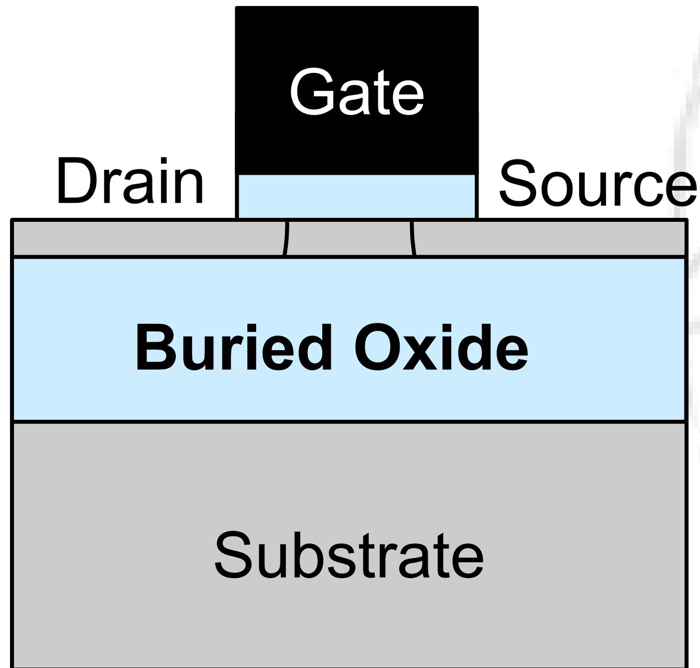
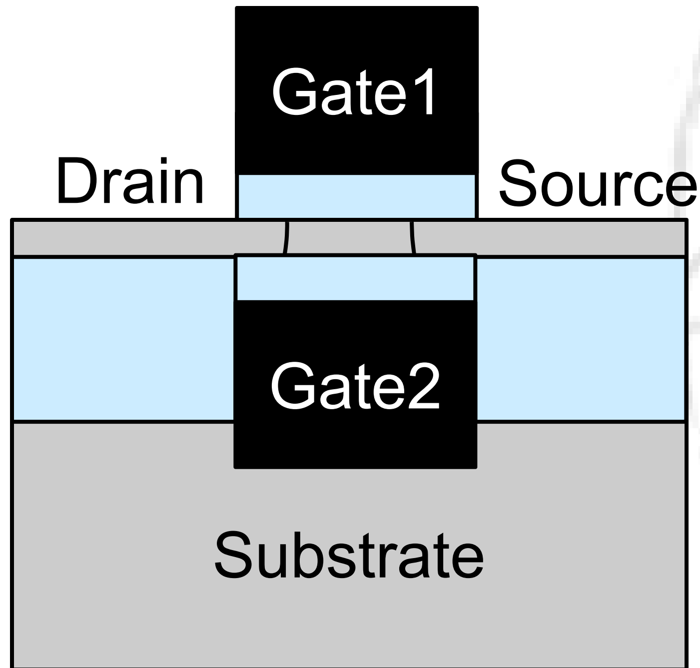


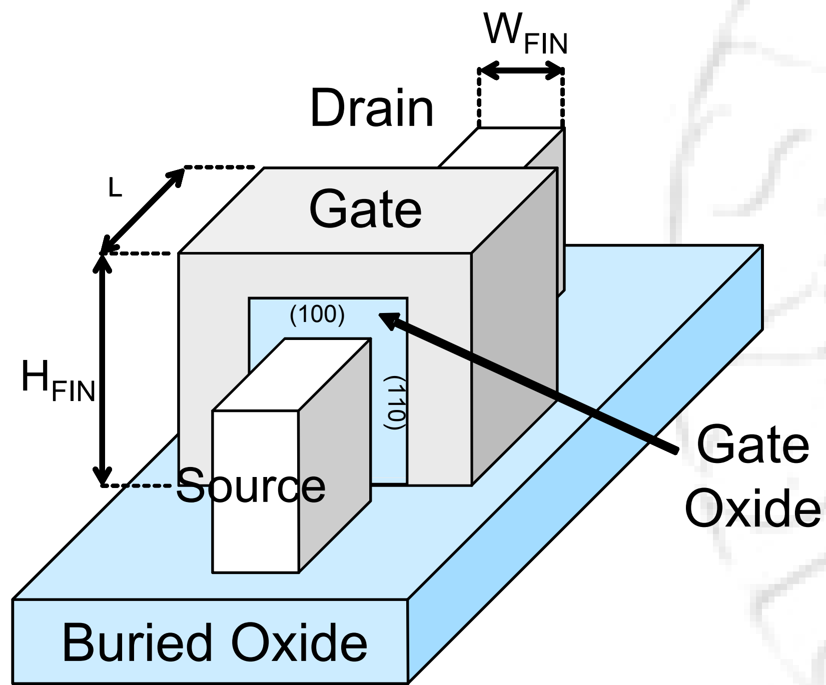
Fully Depleted SOI MOSFET

- Silicon On Insulator (SOI)
  - Partially Depleted
  - Fully Depleted
  - Double Gate
  - FinFETs
- Several Advantages
  - Reduced Capacitance
  - Improved Electrostatics ⇒ Better Short Channel Effects



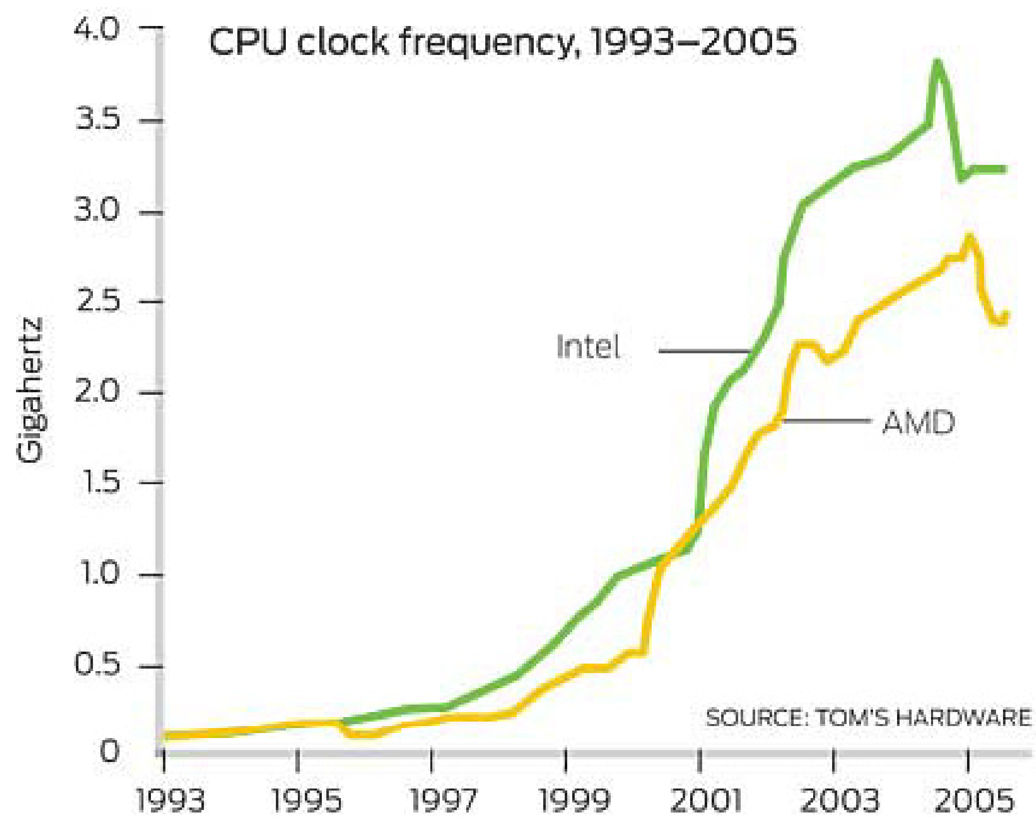
Double Gate SOI MOSFET

- Silicon On Insulator (SOI)
  - Partially Depleted
  - Fully Depleted
  - Double Gate
  - FinFETs
- Several Advantages
  - Reduced Capacitance
  - Improved Electrostatics $\Rightarrow$ Better Short Channel Effects



FinFET

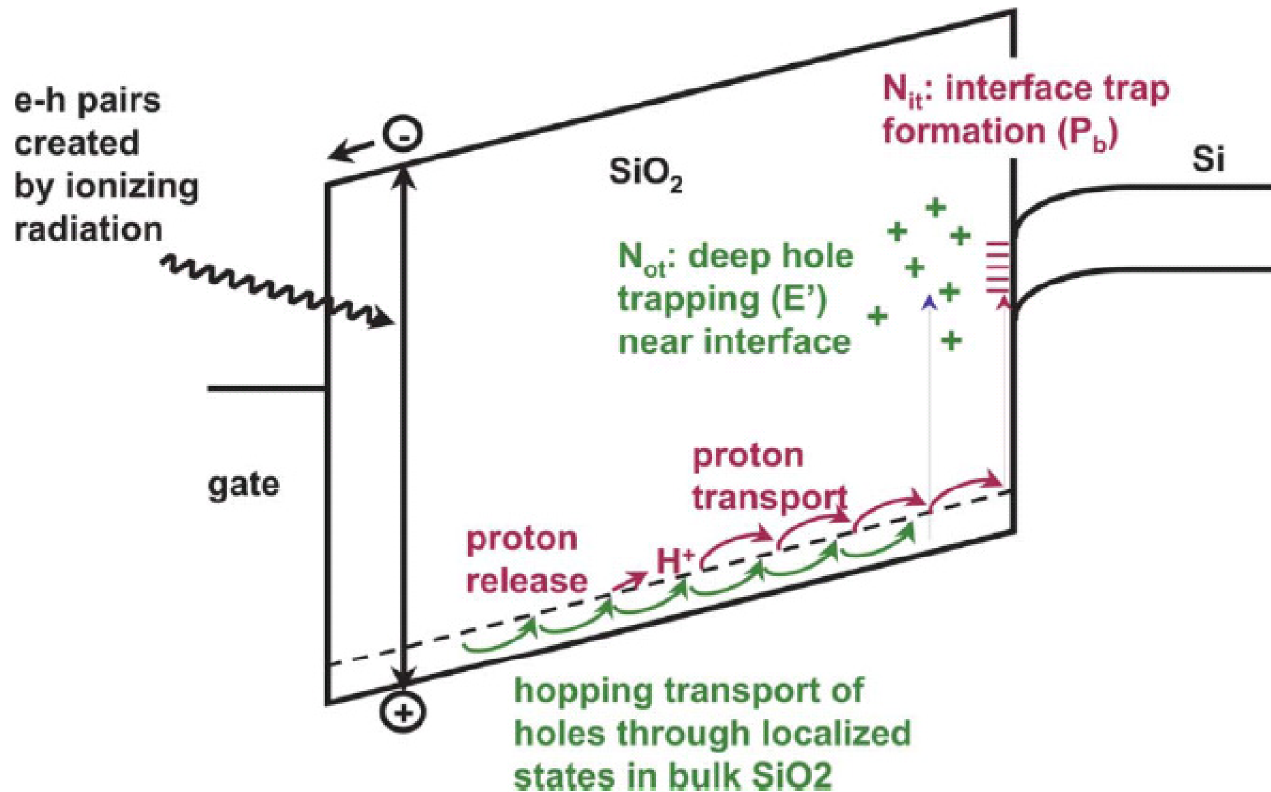
- Silicon On Insulator (SOI)
  - Partially Depleted
  - Fully Depleted
  - Double Gate
  - FinFETs
- Several Advantages
  - Reduced Capacitance
  - Improved Electrostatics $\Rightarrow$ Better Short Channel Effects



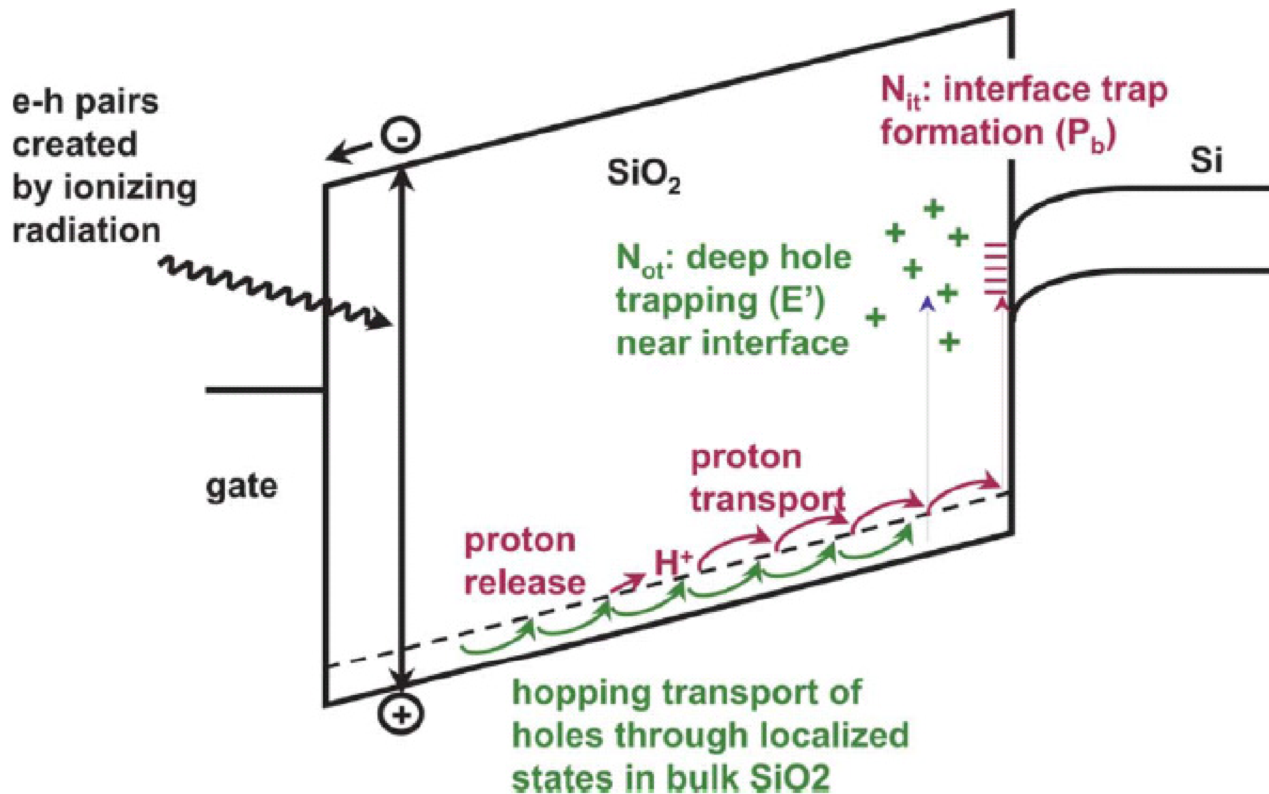
- Until a few years ago, increasing frequency was the focus
- Now, due to power dissipation constraints, parallelism (multi-core CPU) has become the major front

- **Parametric shifts** in transistors parameters due to the build-up of trapped positive charge and interface states caused by several low-LET particles striking a chip

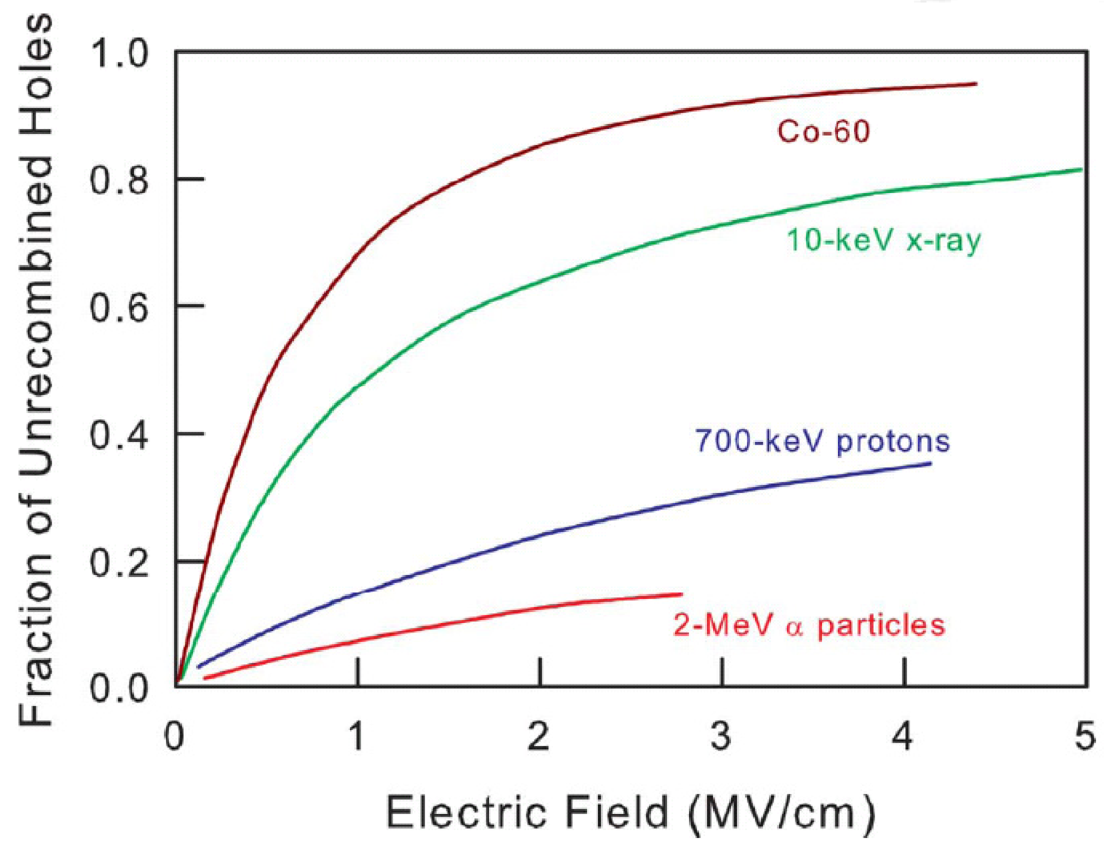
- Total Ionizing Dose affects **dielectric layers** (e.g., gate oxide, isolation oxides)



- Radiation strikes generating **e-h pairs**
- A large part of the e-h pairs **recombine**
- Surviving electrons are quickly swept out of the oxide
- Surviving holes slowly transport in the opposite direction

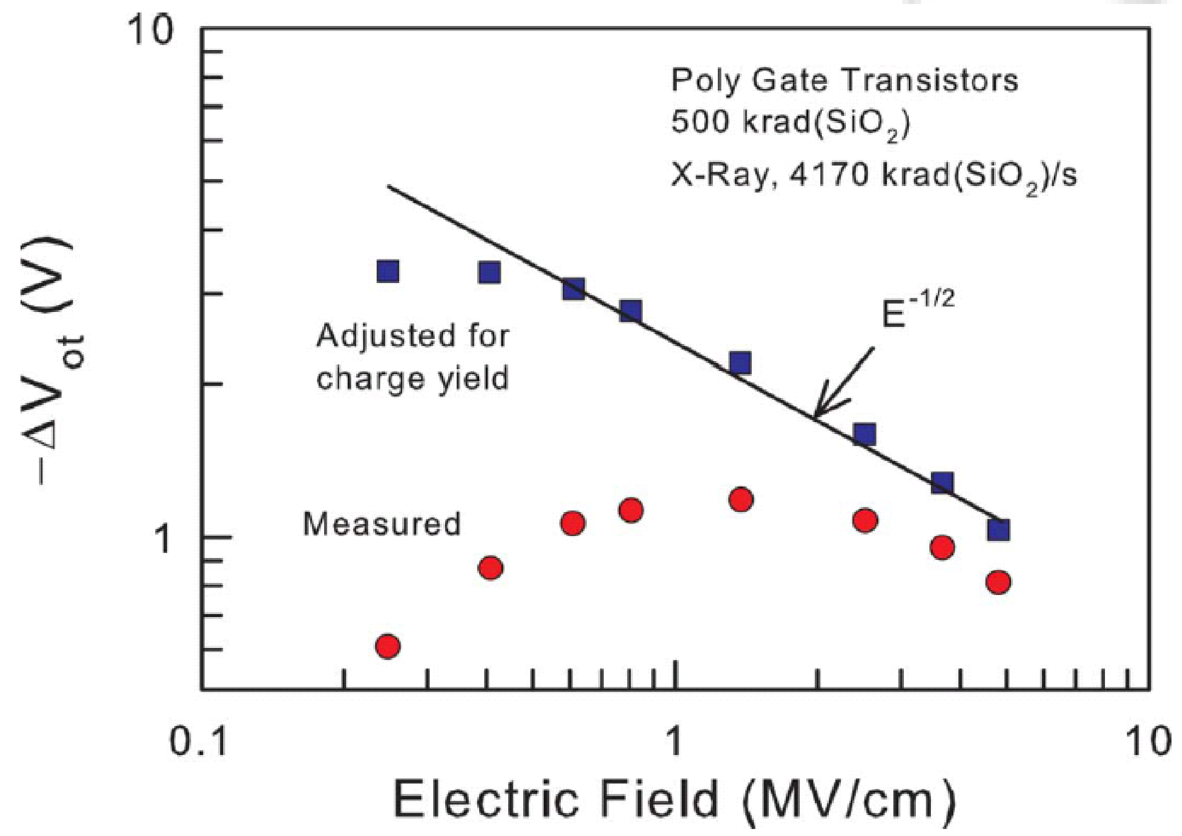


- Holes hop through shallow defects and release **Hydrogen**
- Holes get **trapped** close to the interface
- Hydrogen generates **interface traps**



- A large part of the initial e-h pairs recombine immediately after generation
- Electric field ↑⇒ Charge Yield ↑
- LET ↑⇒ Charge Yield ↓

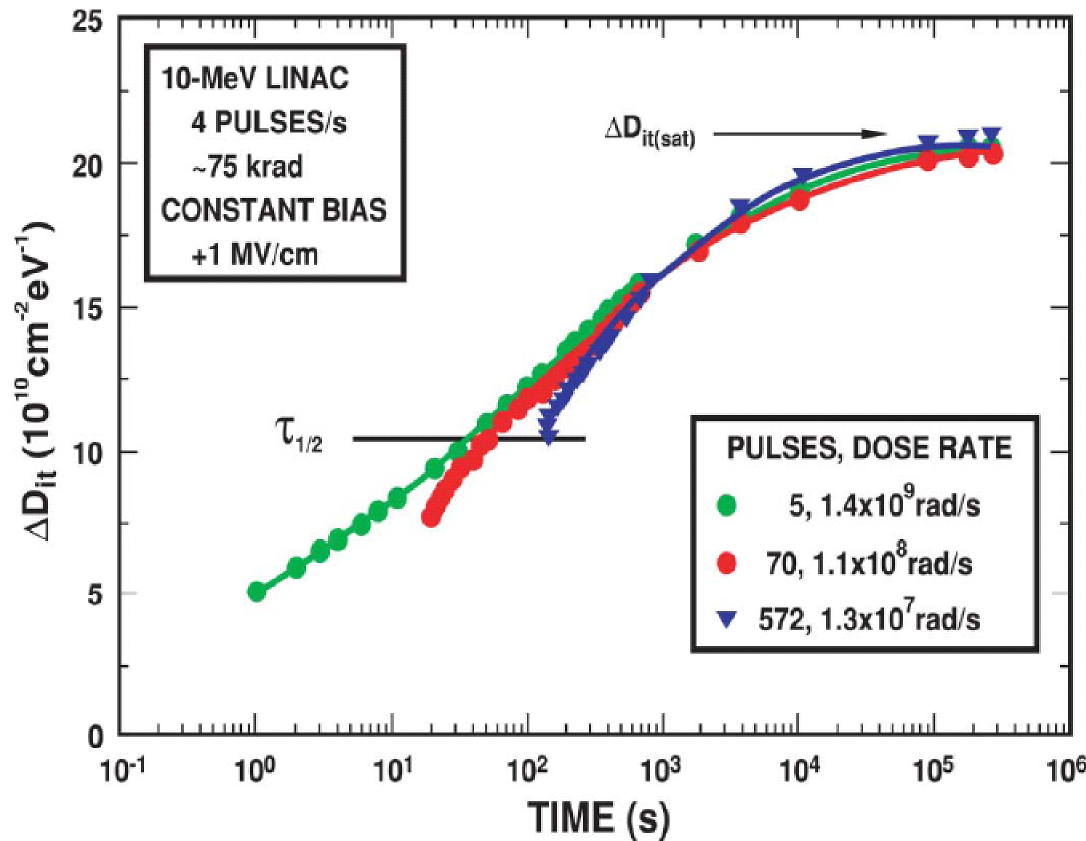
F. B. McLean, et al., Tech. Rep. HDL-TR-2129, 1987.
M. R. Shaneyfelt, et al., IEEE Trans. Nucl. Sci., Dec. 1991.



- Cross section of oxide traps depends on the electric field
- Worst-case bias conditions depend on charge yield and oxide-trap dependence on electric field

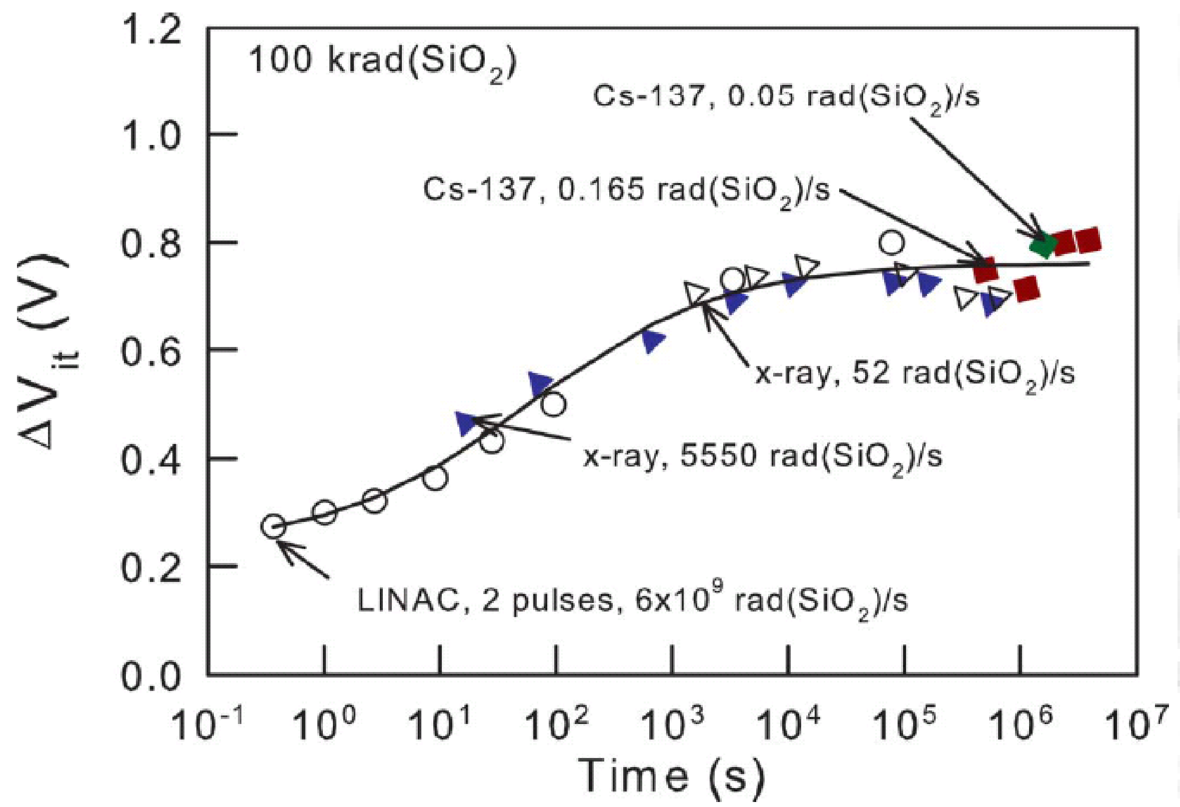
M. R. Shaneyfelt, et al., IEEE Trans. Nucl. Sci., 1990

Interface States vs Time



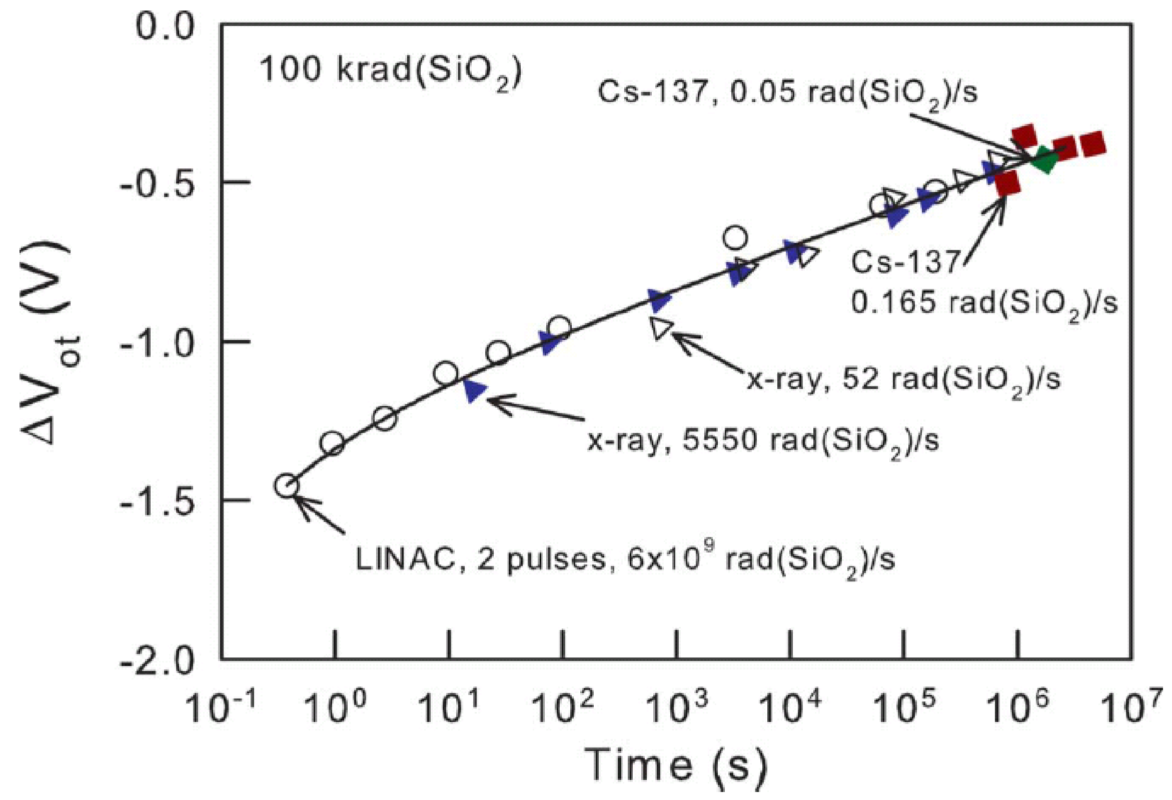
M. R. Shaneyfelt, et al., IEEE Trans. Nucl. Sci., 1992.

- Interface trap generation occurs over time, after radiation exposure, due to holes and Hydrogen transport to the interface
- Bias conditions play a fundamental role



- No true dose-rate dependence
- Given equal time from the irradiation, the same amount of interface state and trapped charge will occur, regardless of dose rate

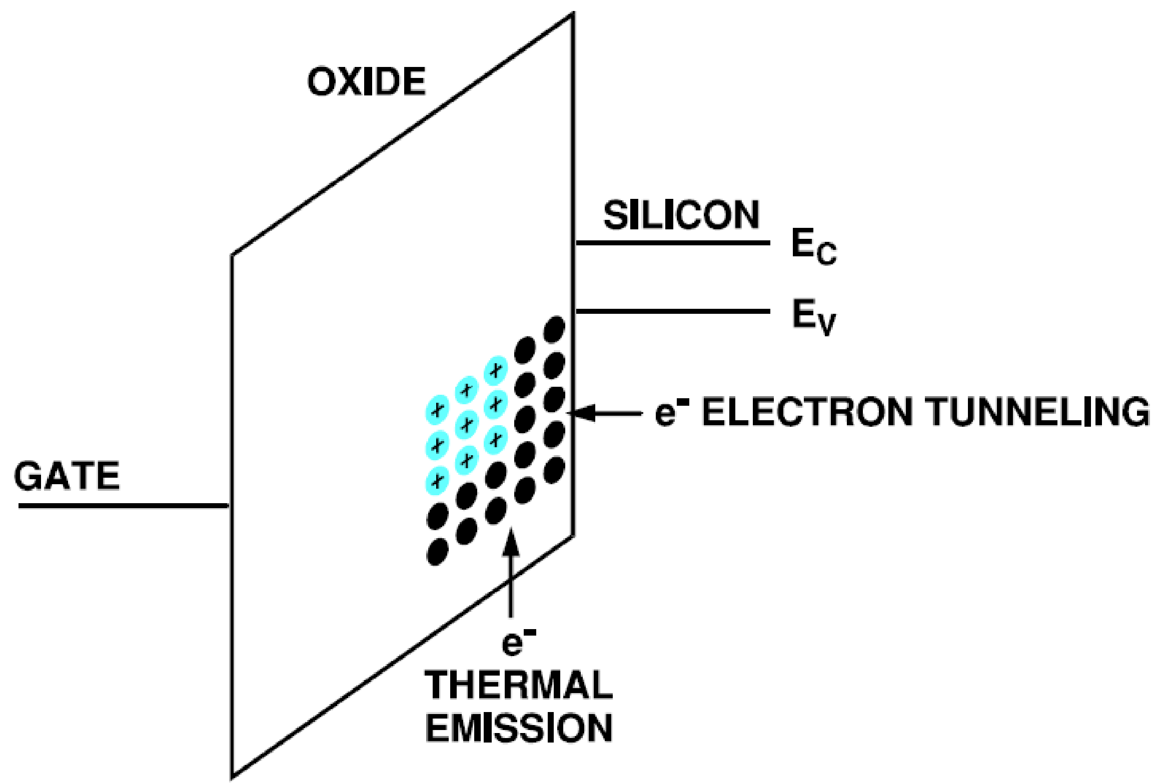
D. M. Fleetwood, et al., IEEE Trans. Nucl.1988.



- Trapped charge changes over time
- No dose-rate effects

D. M. Fleetwood, et al., IEEE Trans. Nucl.1988.

Annealing Mechanisms



P. J. McWhorter, et al., IEEE Trans. Nucl. Sci., 1990.

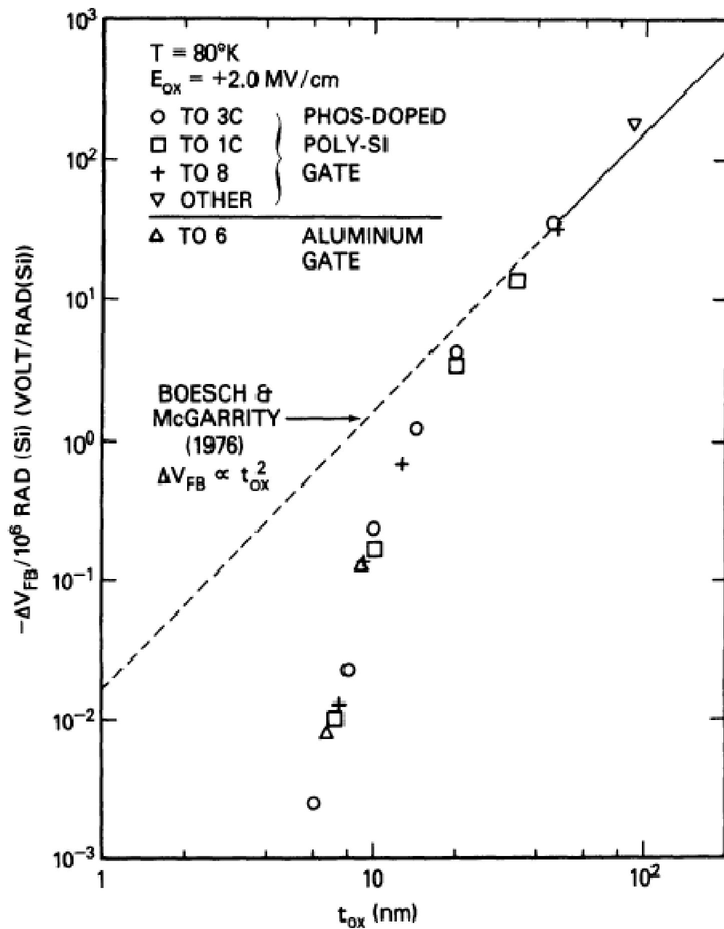
- Neutralization of trapped holes due
  - Tunneling
  - Thermal Emission
- Annealing of interface traps does not occur at room temperature

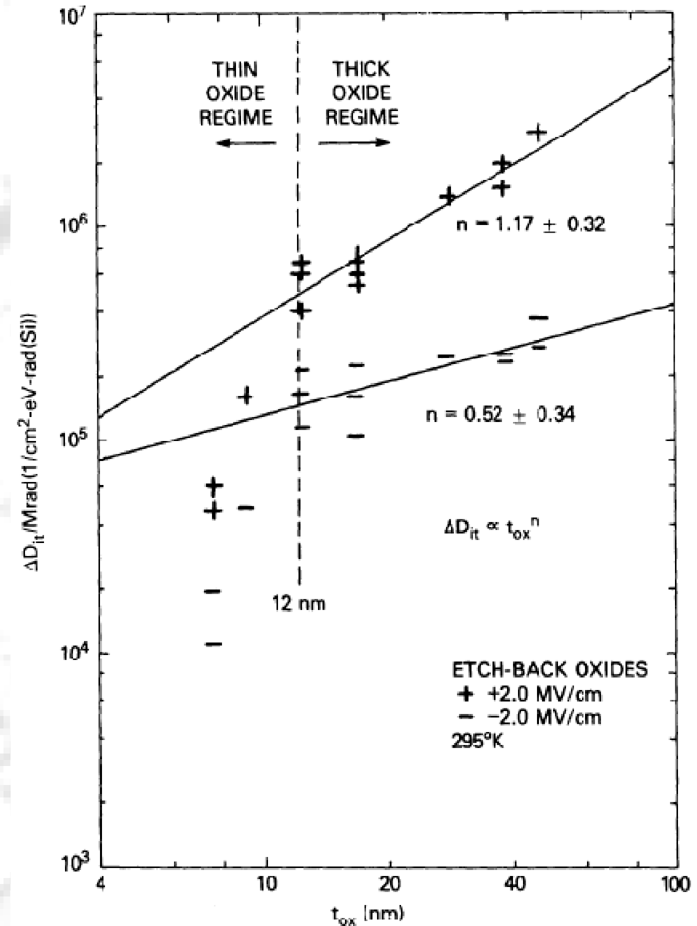
Oxide Thickness Scaling

- Simple model for charge trapping dependence on oxide thickness:

$$\Delta V_t = Q_{ot}/C_{ox} = k \cdot t_{ox}^2$$

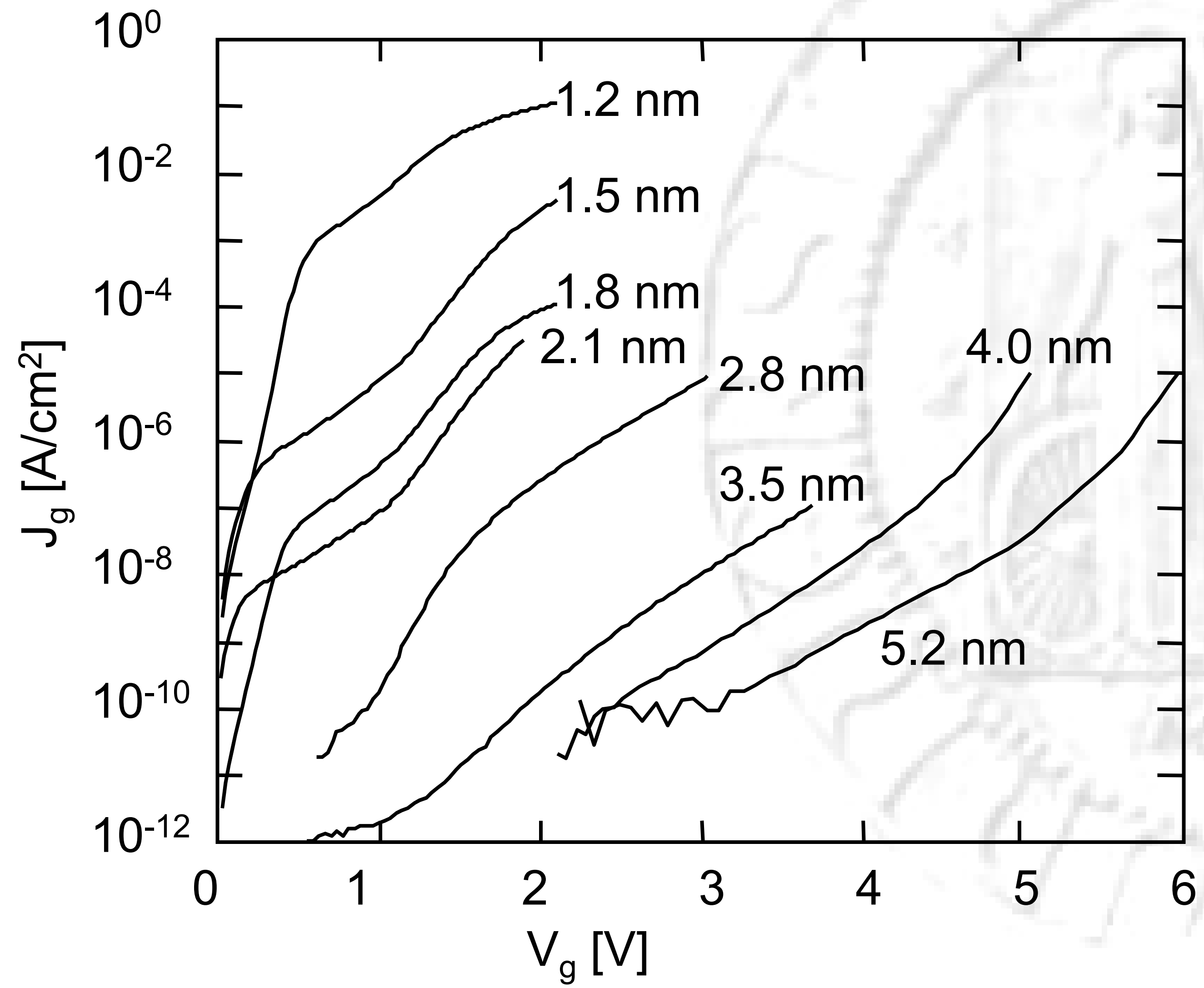
- The thinner the oxide, the smaller the degradation
- Actually, things go even better for ultra-thin oxides (< 10 nm)…





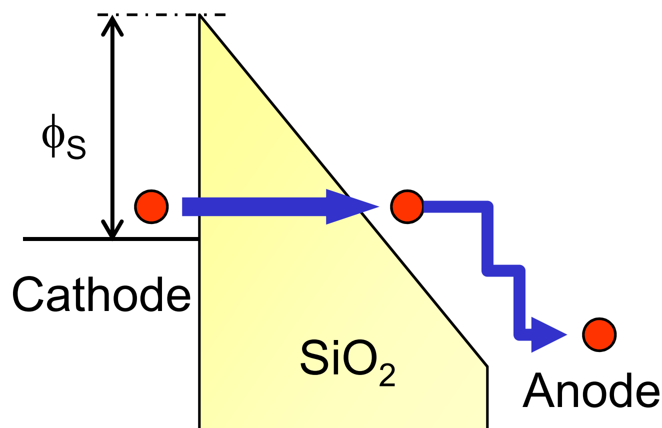
Saks and Ancona, 1986

- Rapidly decreasing charge trapping and interface state formation in ultra-thin oxides



- Fowler-Nordheim tunneling
- Direct tunneling
- Leakage is a limit to scaling

D.J. Frank et al., Proc. IEEE, 2001



Electron tunneling through a triangular barrier

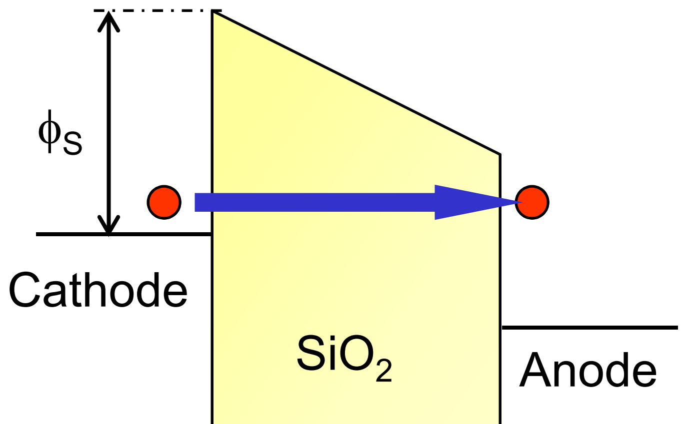
$$J_{FN} = A \cdot E_{ox}^{2} \cdot \exp\left(-\frac{B}{E_{ox}}\right)$$

$$A = \frac{q^3 \cdot m_o}{16\pi^2 \cdot \hbar \cdot m_{ox} \cdot \phi_S}$$

$$B = \frac{4 \cdot \sqrt{2 \cdot m_{ox}} \cdot \phi_S^{3/2}}{3 \cdot \hbar \cdot q}$$

R. Fowler and L. Nordheim, Proc. Roy. Soc. A, 1928

Electron tunneling through a trapezoidal barrier

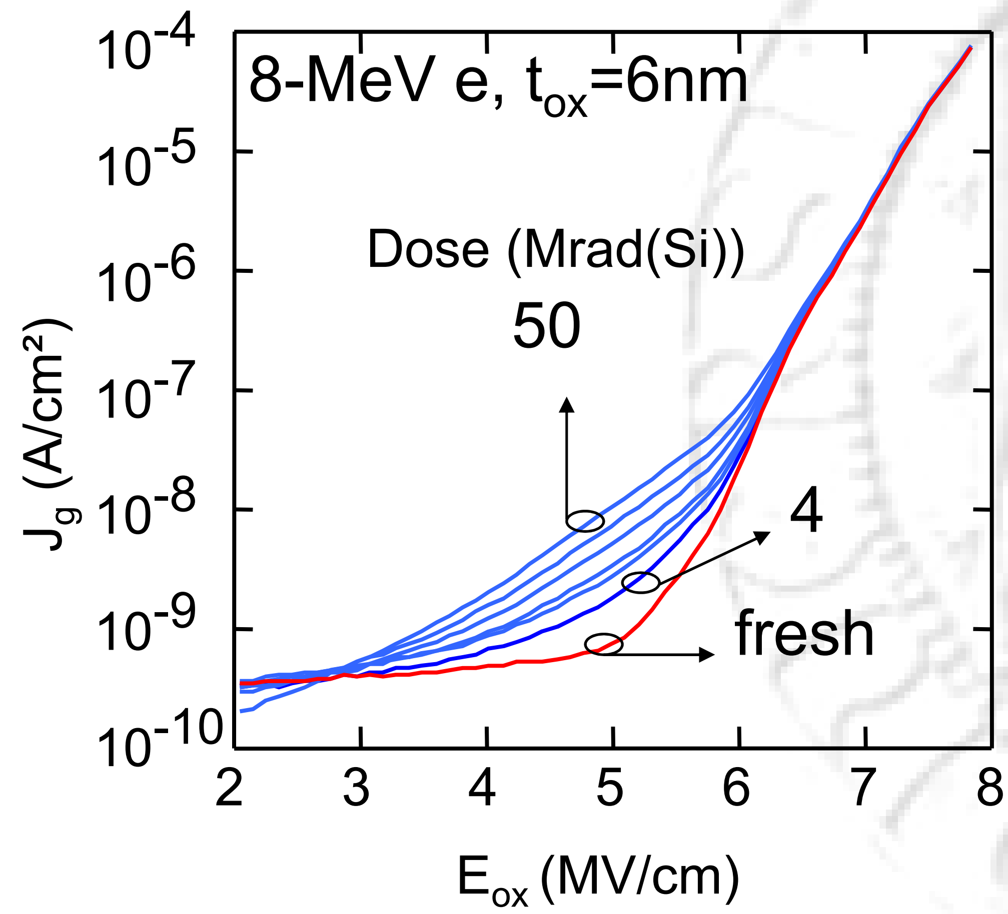


$$B = \frac{4 \cdot \sqrt{2 \cdot m_{ox}} \cdot \phi_S^{3/2}}{3 \cdot \hbar \cdot q}$$

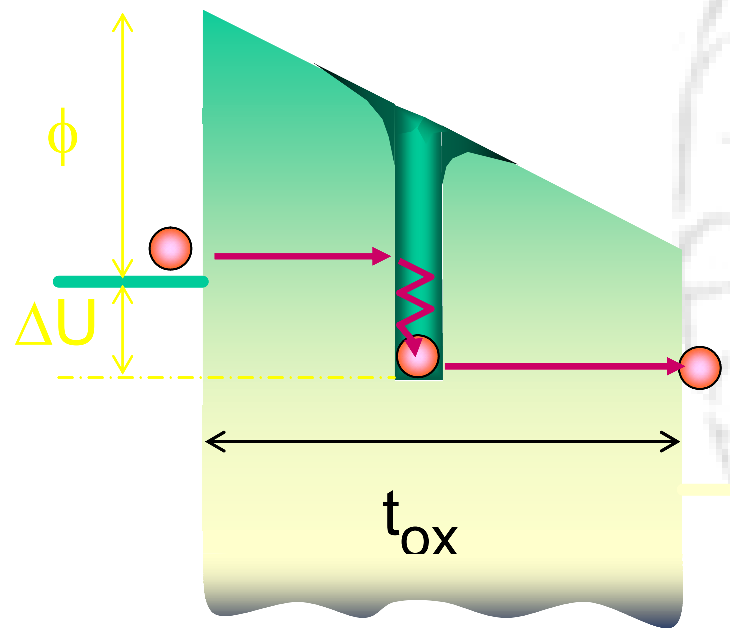
$$A = \frac{q^3 \cdot m_o}{16\pi^2 \cdot \hbar \cdot m_{ox} \cdot \phi_S}$$

$$J_D = \frac{A \cdot E_{ox}^2}{\left(1 - \sqrt{\frac{\phi_S - q \cdot E_{ox} \cdot t_{ox}}{\phi_S}}\right)^2} \cdot \exp\left[-\frac{B}{E_{ox}} \cdot \frac{\phi_S^{3/2} - (\phi_S - q \cdot E_{ox} \cdot t_{ox})^{3/2}}{\phi_S^{3/2}}\right]$$

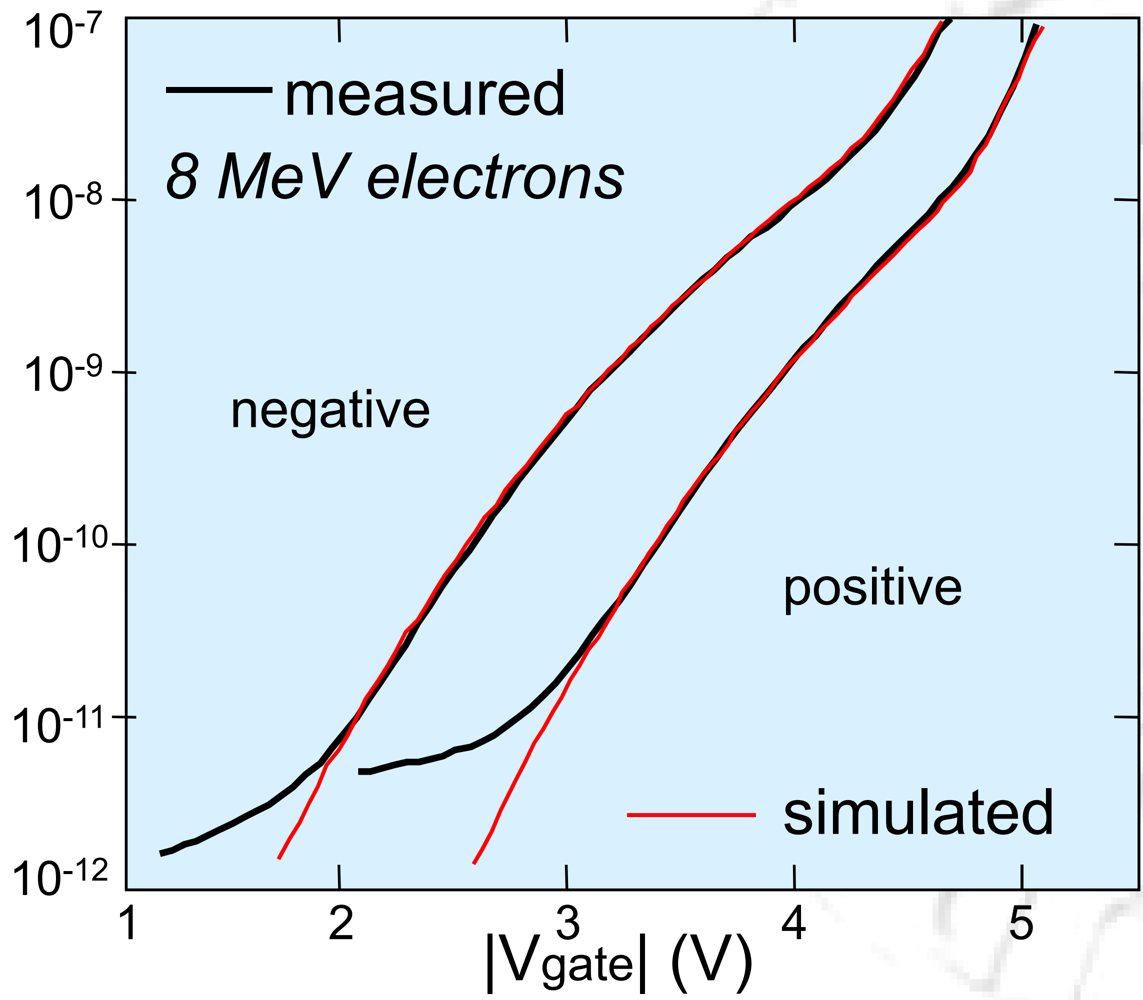
Wentzel-Kramers-Brillouin (WKB) approximation



- When t_{ox}<7 nm irradiation induces leakage current at low fields
- **Radiation Induced Leakage Current (RILC)**
- True DC conduction
- Not depending on radiation LET



- Radiation induced defects: electron neutral traps
- Conduction mechanism: inelastic electron Trap Assisted Tunneling (TAT)
- Modeled by WKB or other methods
- Oxide field dependent
- Most effective RILC defects at $\approx t_{ox}/2$
- Generation mechanism correlated to the trapped positive charge

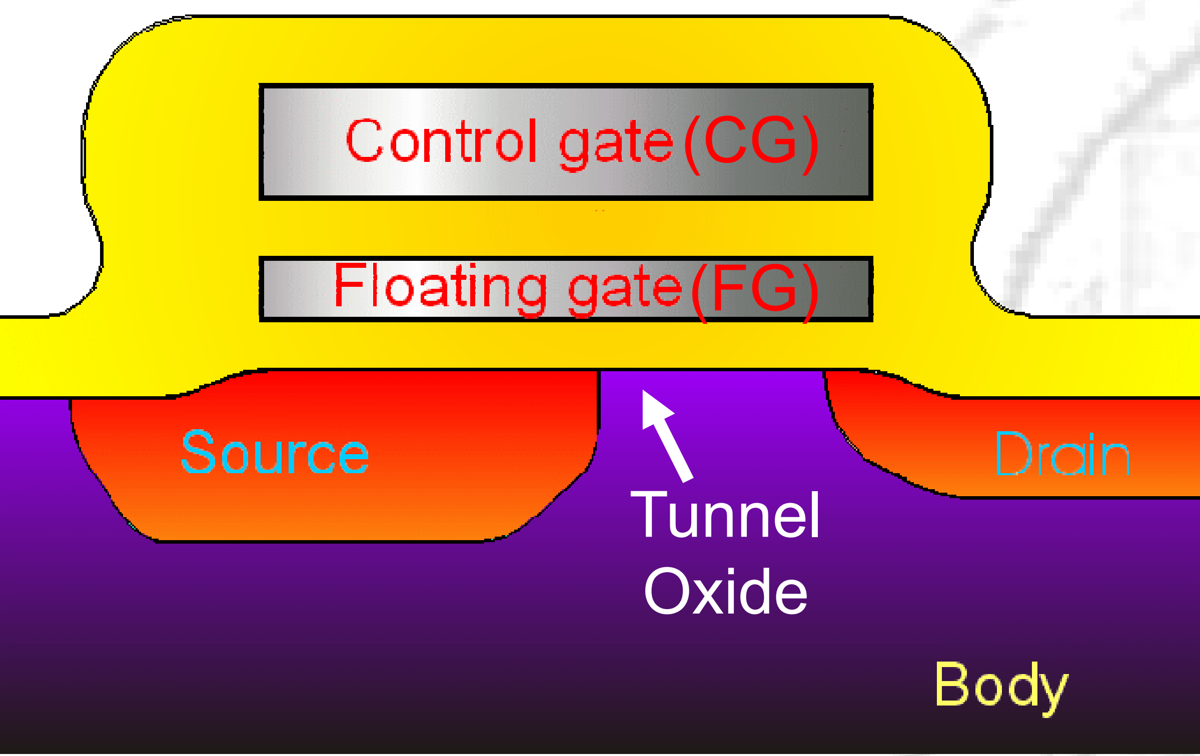


Defect characteristics:

- 1.3 eV below oxide Ec
- Density proportional to dose
- Independent of radiation LET (for low LET)

L. Larcher et al., IEEE-TNS, 1999

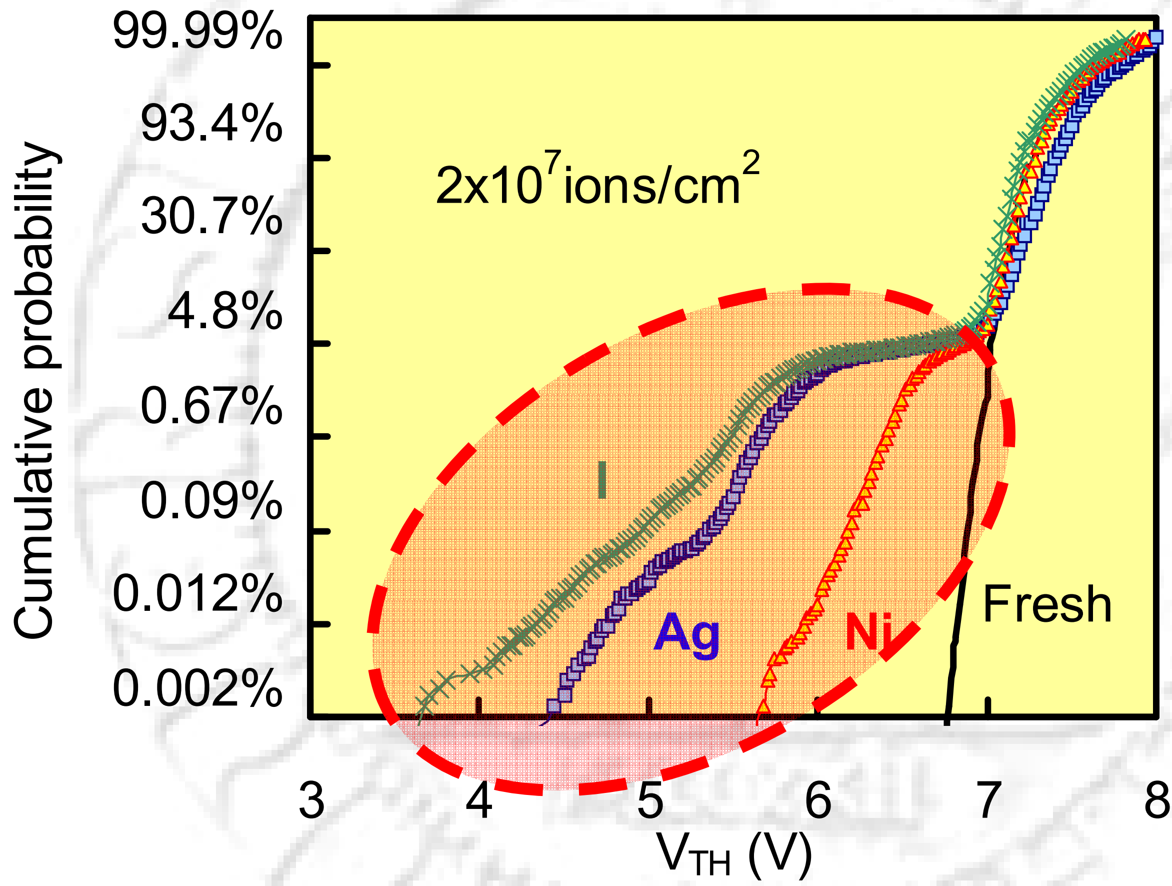
Floating Gate Memories



- Electrons stored in the FG
  → V_{TH} grows
- Writing (Flash):
  - Channel Hot Electron tunnelling
- Erasing (Flash):
  - Fowler-Nordheim tunnelling

Main reliability issues:
- Endurance (W/R/E cycles)
- Data retention

- Large tails after heavy ions irradiation
- Number of bits in tail does not depend on ion LET (only on fluence)
- ΔV_{TH} strongly depends on ion LET

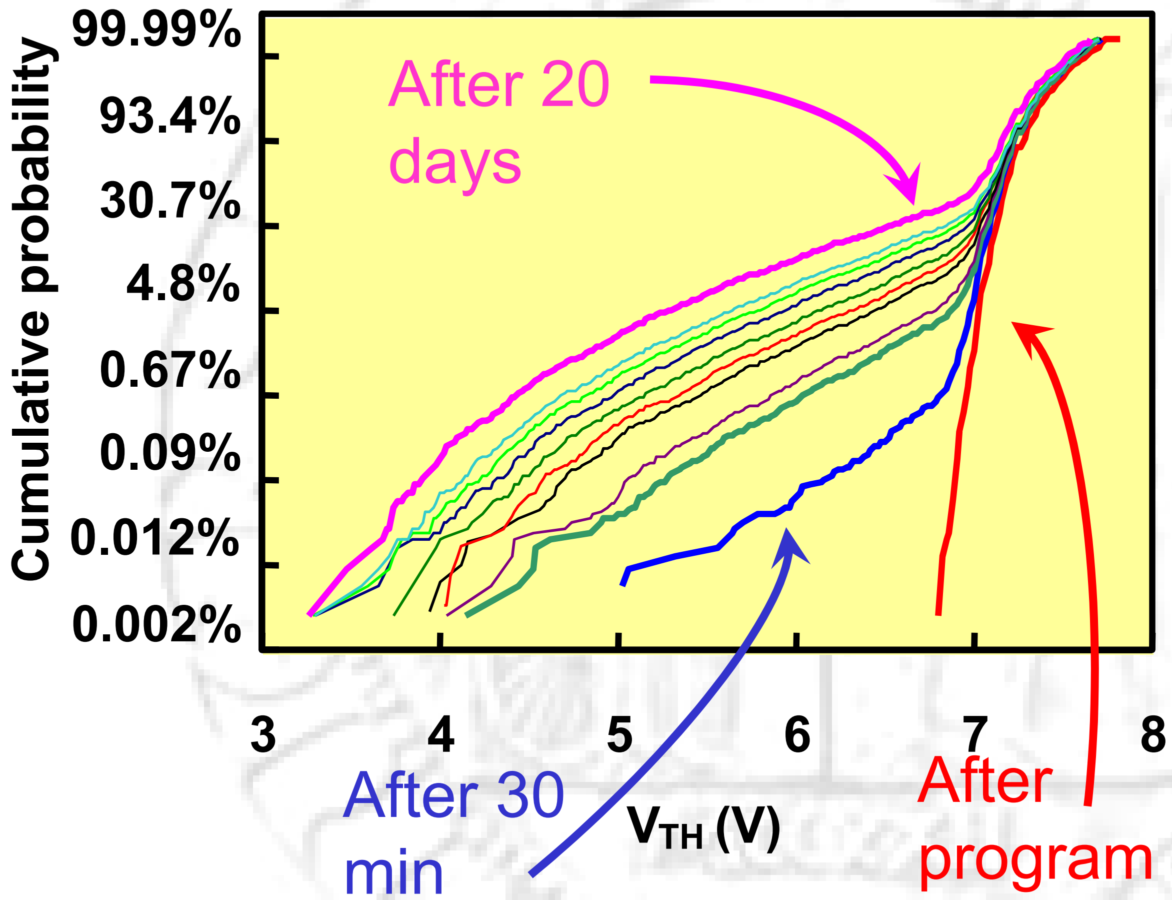


- Only hit cells are considered in next experiments

Cellere et al, T-NS, 2003, 2004, and APL, 2005

Long-term Effects

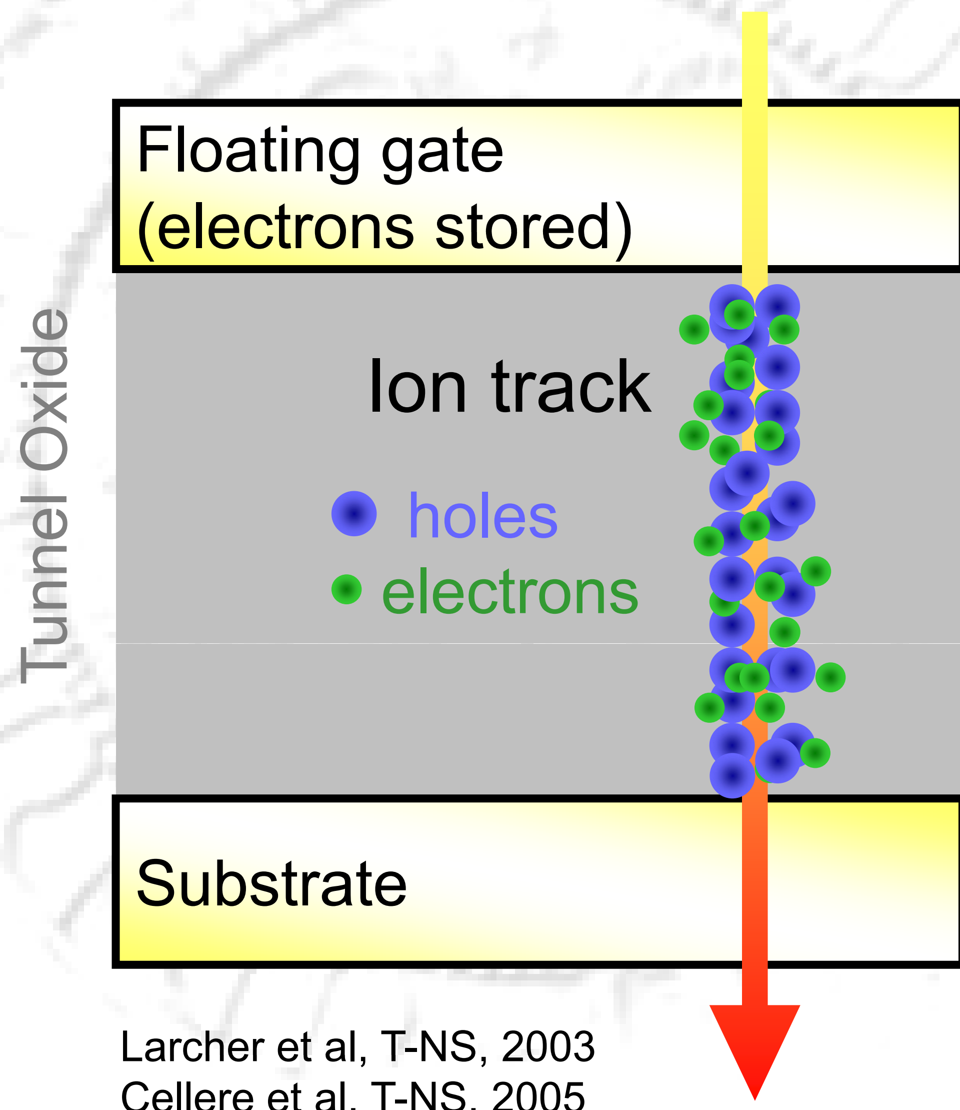
- Only hit FGs were programmed
- After only 30min a clear tail appears…
- …which increases more and more with time



Cellere et al, T-NS, 2003, 2004, and APL, 2005

RILC (Radiation Induced Leakage Current)

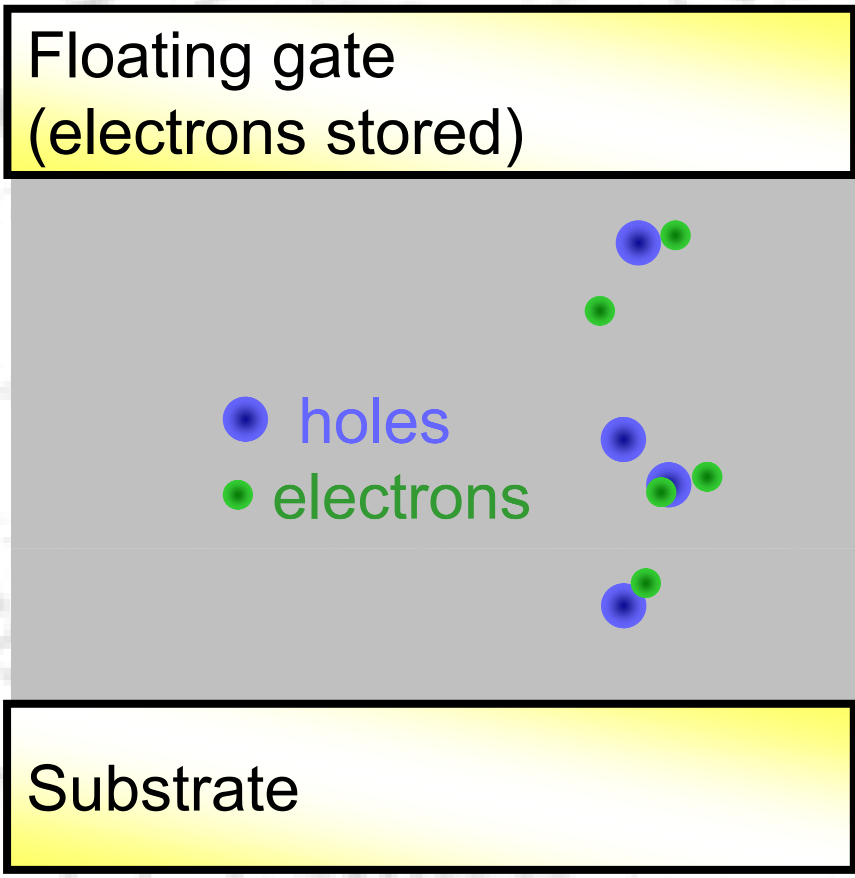
- What's going on?
  - Ion generates a plasma of electrons and holes



Larcher et al, T-NS, 2003
Cellere et al, T-NS, 2005

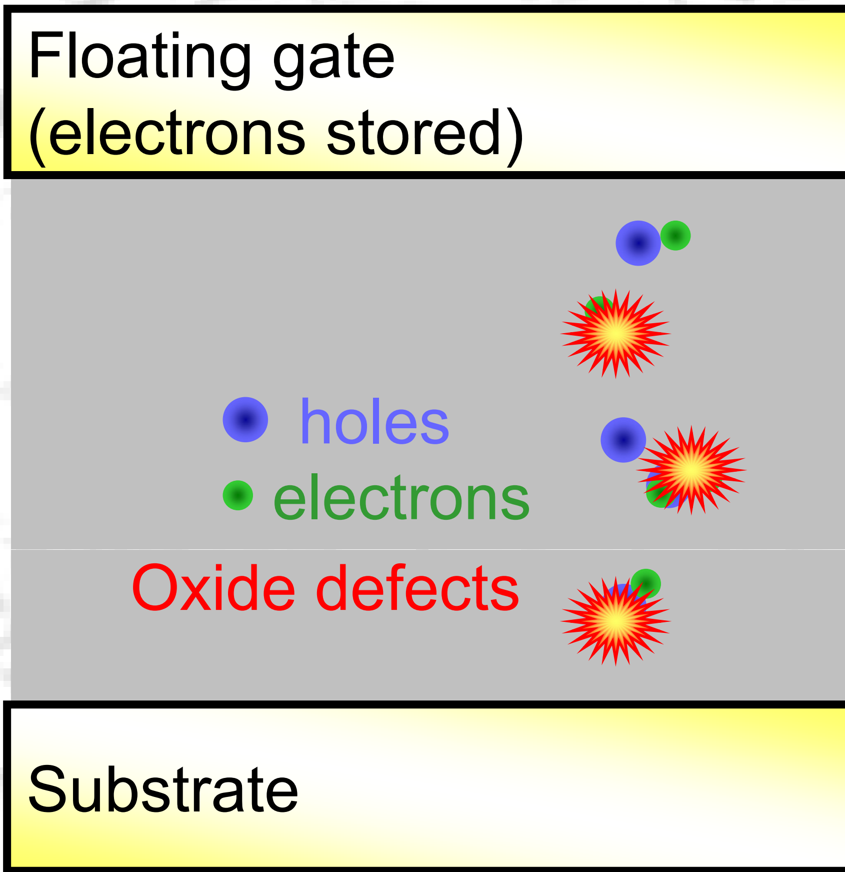
What's going on?

- Ion generates a plasma of electrons and holes
- Prompt columnar recombination



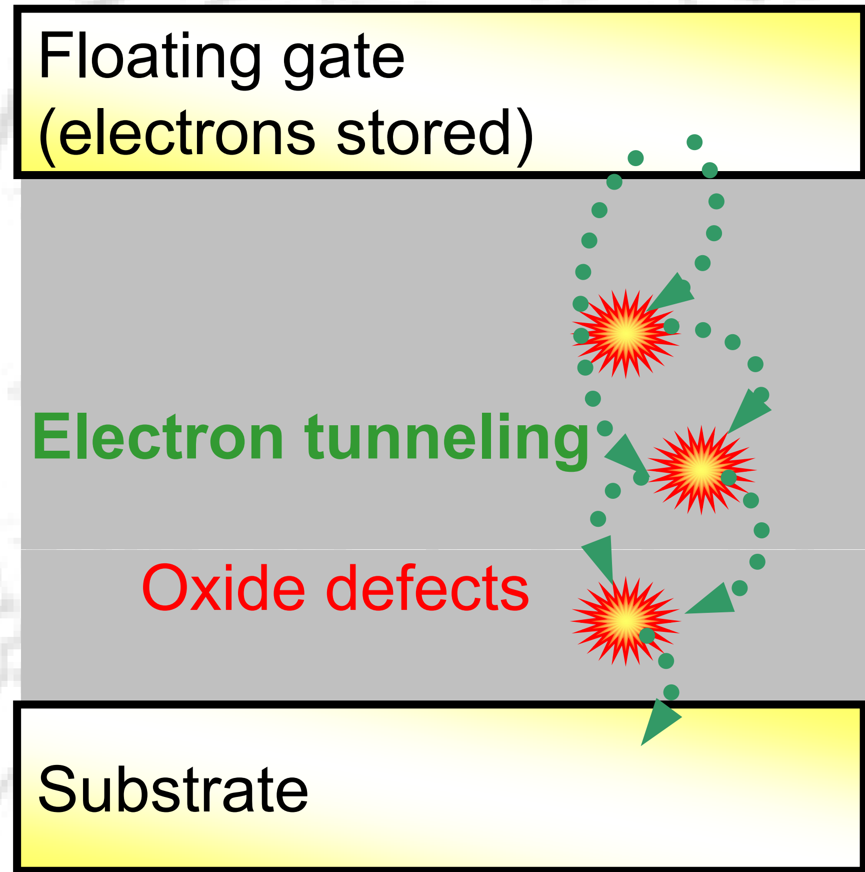
Larcher et al, T-NS, 2003
Cellere et al, T-NS, 2005

- What's going on?
  - Ion generates a plasma of electrons and holes
  - Prompt columnar recombination
  - Followed/accompanied by generation of oxide defects



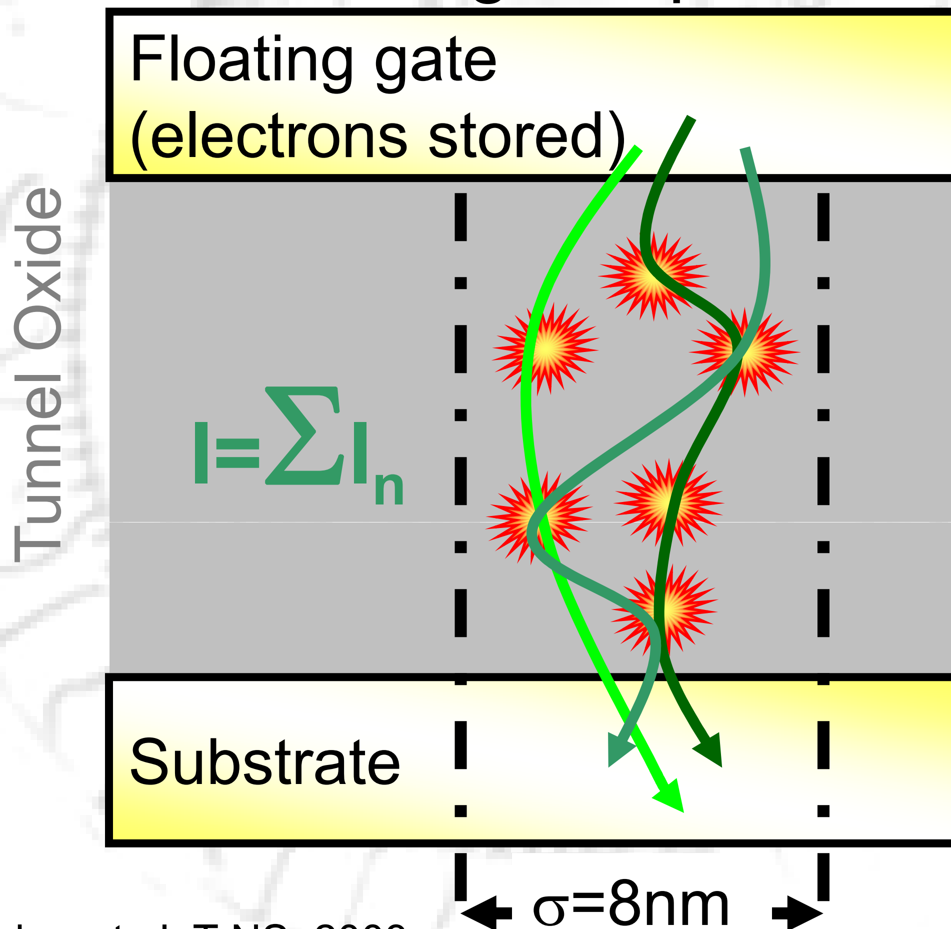
Larcher et al, T-NS, 2003
Cellere et al, T-NS, 2005

- What's going on?
  - Ion generates a plasma of electrons and holes
  - Prompt columnar recombination
  - Followed/accompanied by generation of oxide defects
- Oxide defects are used by electrons to escape the FG
  - multi-Trap Assisted Tunneling (m-TAT)



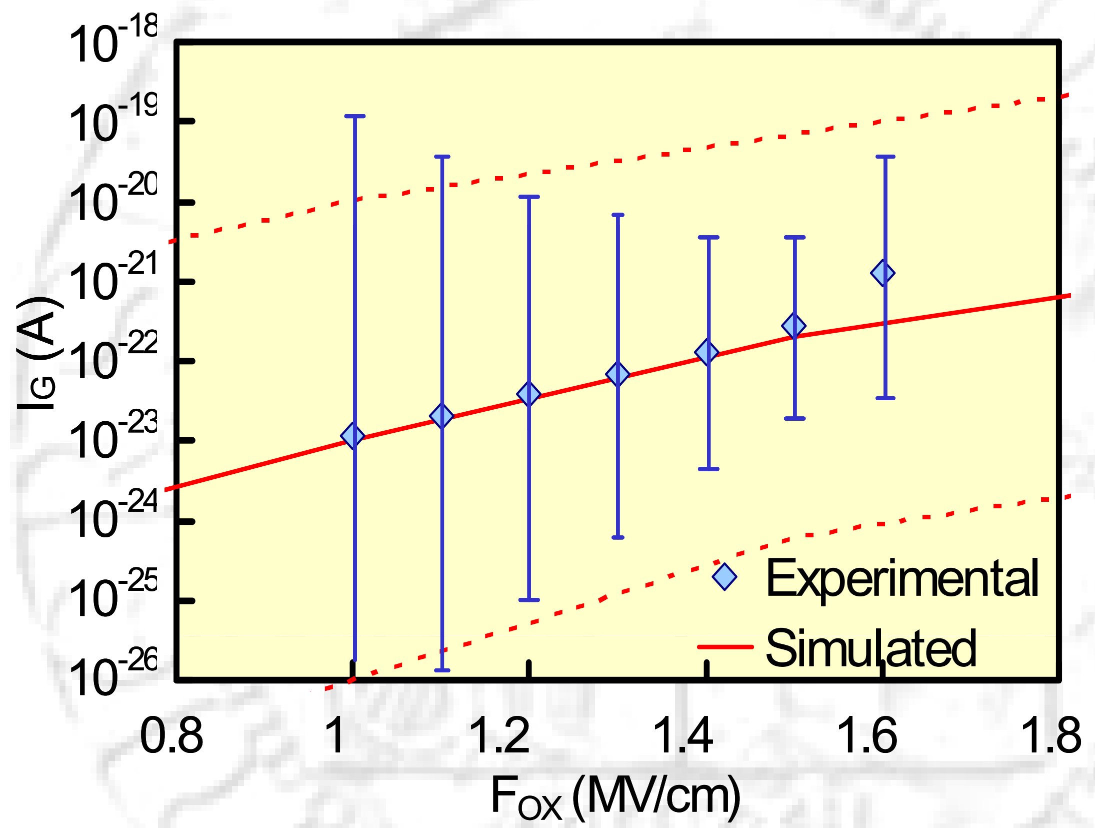
Larcher et al, T-NS, 2003
Cellere et al, T-NS, 2005

- How can we evaluate the current along this path?
- Consider the ion track
- Randomly generate a Gaussian distribution of defects
- Evaluate the current through each possible path (phonon-assisted)
- Then sum all the currents



Larcher et al, T-NS, 2003
Cellere et al, T-NS, 2005, 2006

- Symbols → average, experimental data
- Bars → variance (spread) of experimental data
- Lines → calculations

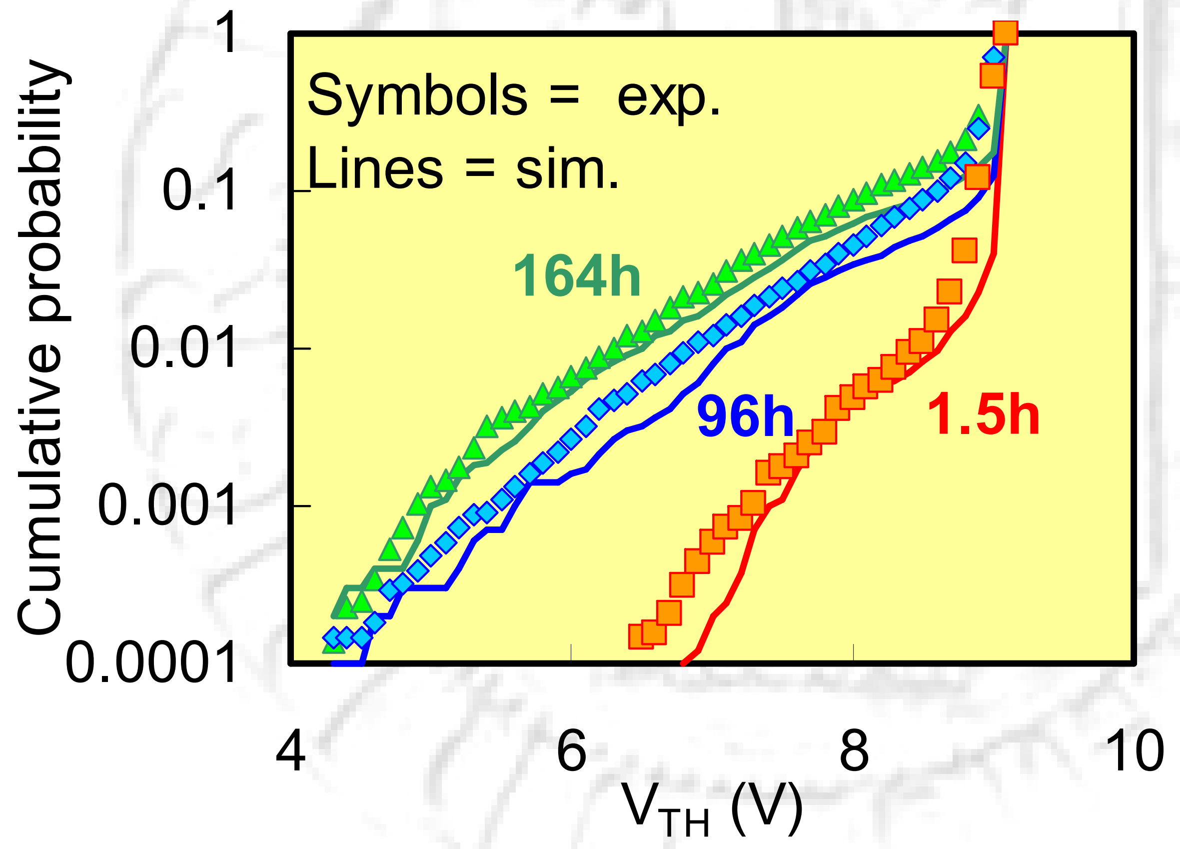


Current as low as 10^{-24}A → 1n(fA)

Larcher et al, T-NS, 2003

- Once coupled with a model of the FG cell, the leakage model can be used to derive the V_{TH} evolution over time

- After Iodine (LET=64 $MeVcm^2/mg$) irradiation



Cellere et al, T-NS, 2005

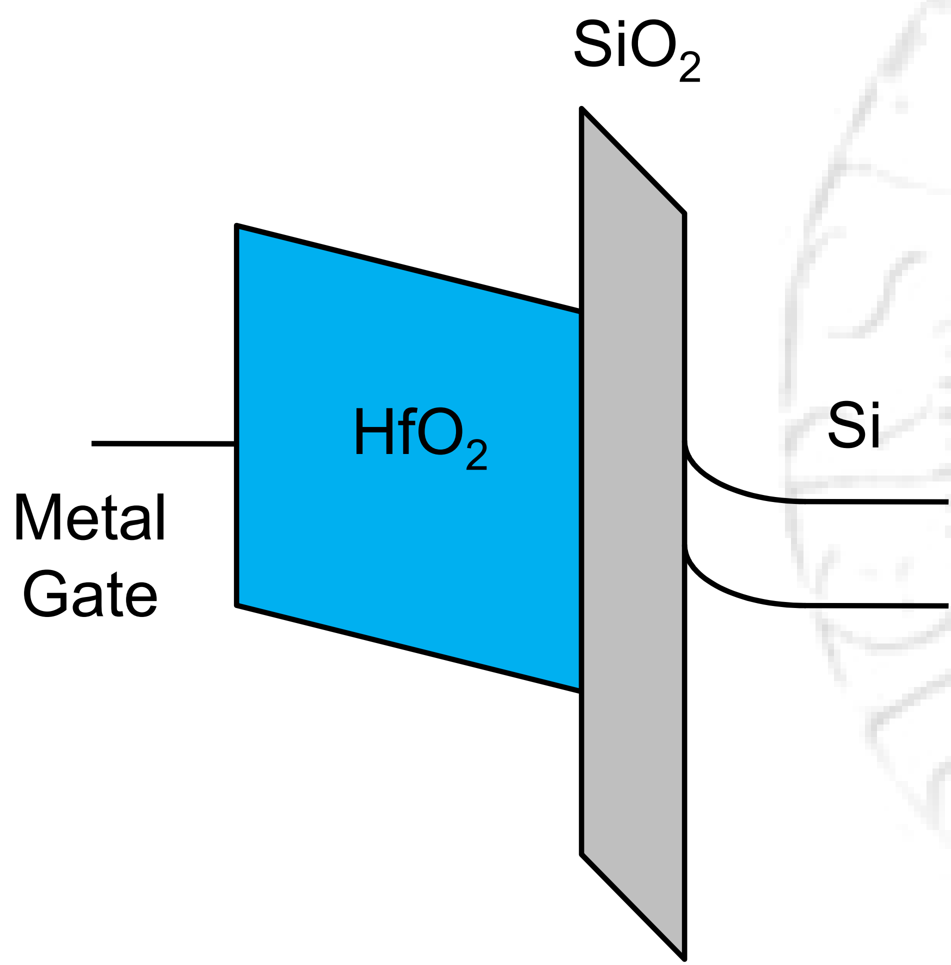
Why Nitrided Oxides?

- Improve dielectric constant
- Reduce leakage current
- Prevent boron penetration
- Better hot carrier reliability

Radiation Hardness

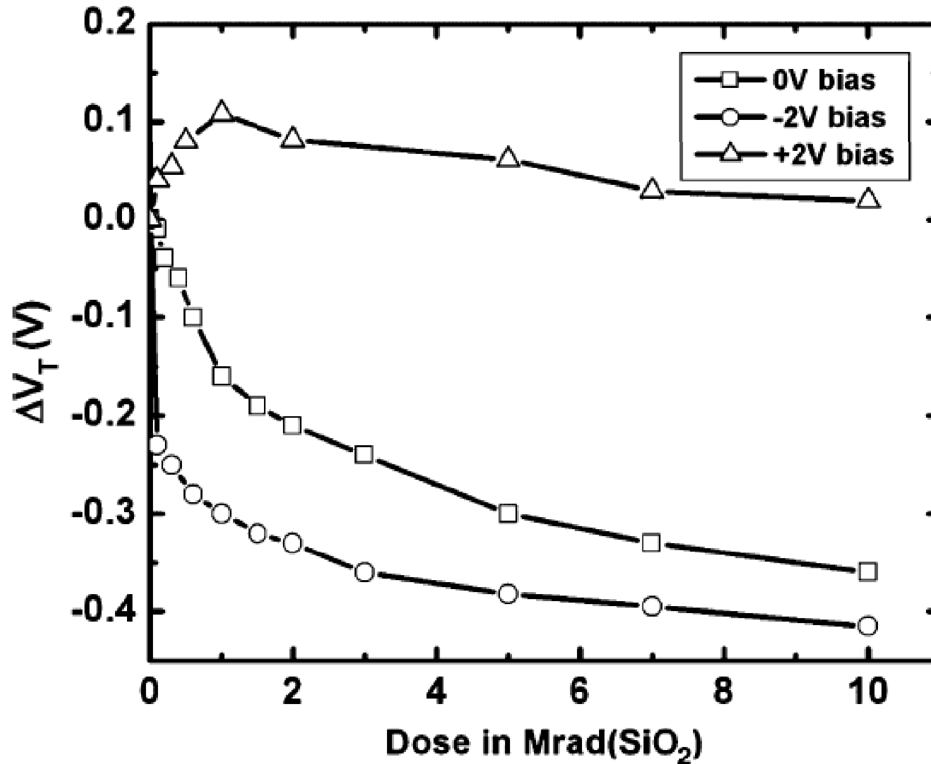
- Suppression of interface states, Nitrogen layer acts as a barrier for Hydrogen diffusion
- Comparable density of oxide charge-traps in SiON and SiO_2

High-k Gate Oxides



- Research on radiation effects in high-k oxides far less advanced than in SiO_2
- Different Band Structure
  - Smaller bandgap ⇒ less energy for e-h pair generation
  - Recombination, Charge Yield?
  - Pre-existing defects
  - Different barriers ⇒ different carrier tunneling probabilities

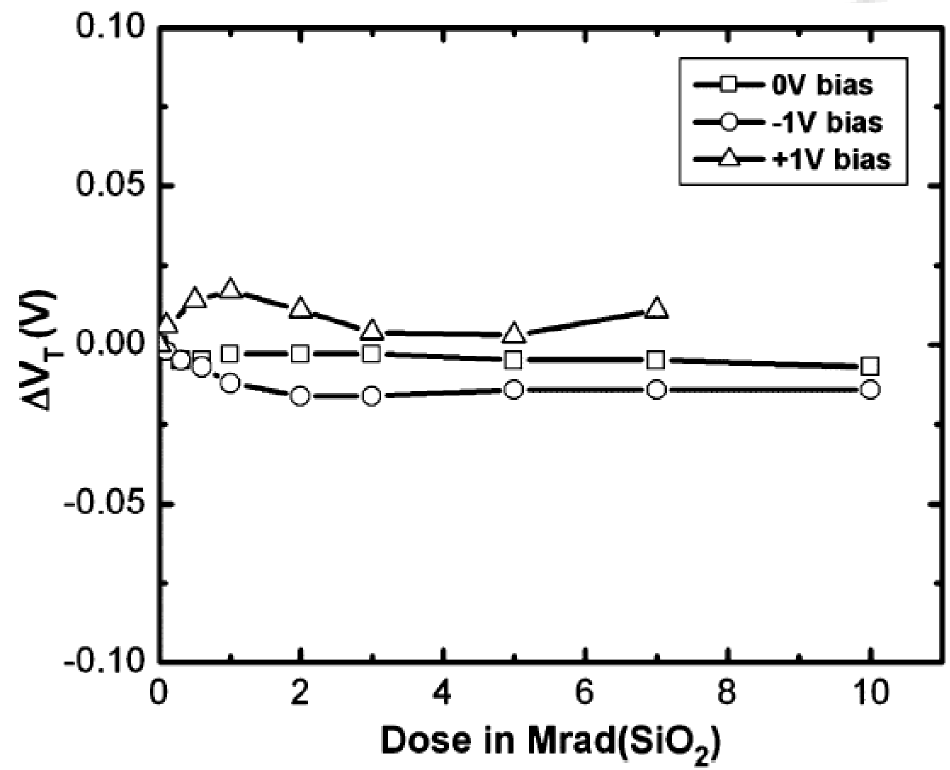
Thick High-k Gate Oxides



Gate oxide:1nm SiO_2 + **7.5nm** HfO_2 EOT = **2.3nm**

S. K. Dixit, et al., IEEE Trans. Nucl. 2007.

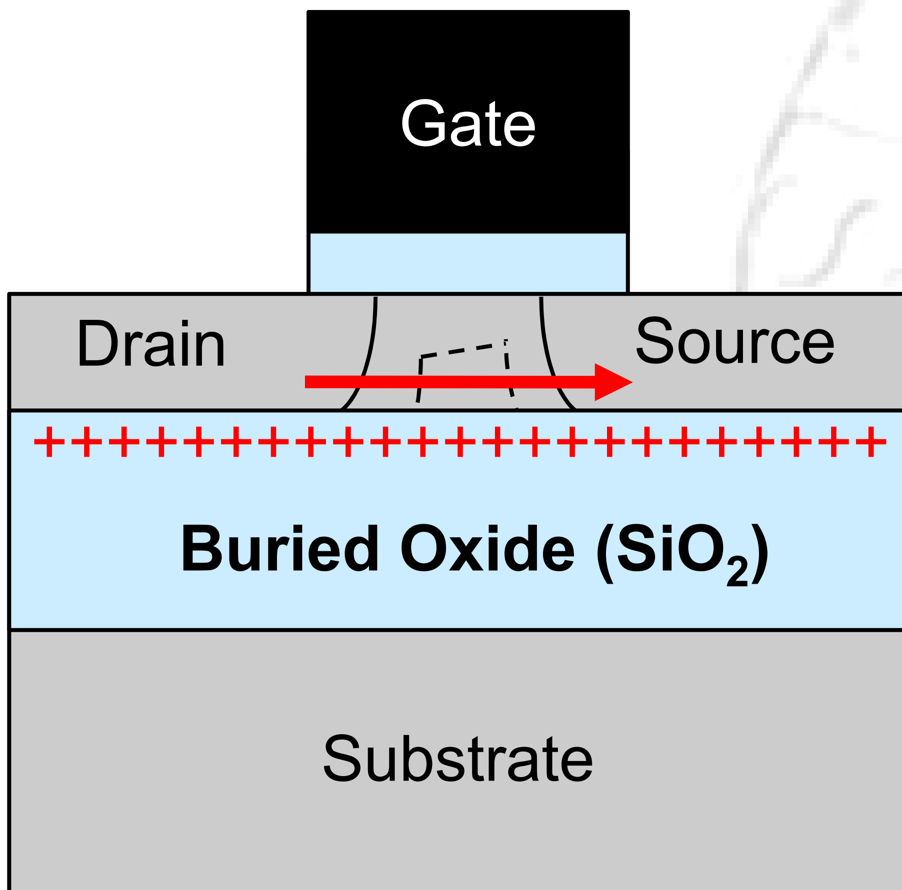
- Thicker oxides, a return to charge trapping?
- Significant number of **electron traps** in HfO_2 in addition to hole traps
- **Minimal** charge trapping for thin HfO_2 with buffer SiO_2 layer



Gate oxide:1nm SiO_2 + **3.0nm** HfO_2 EOT = **1.5nm**

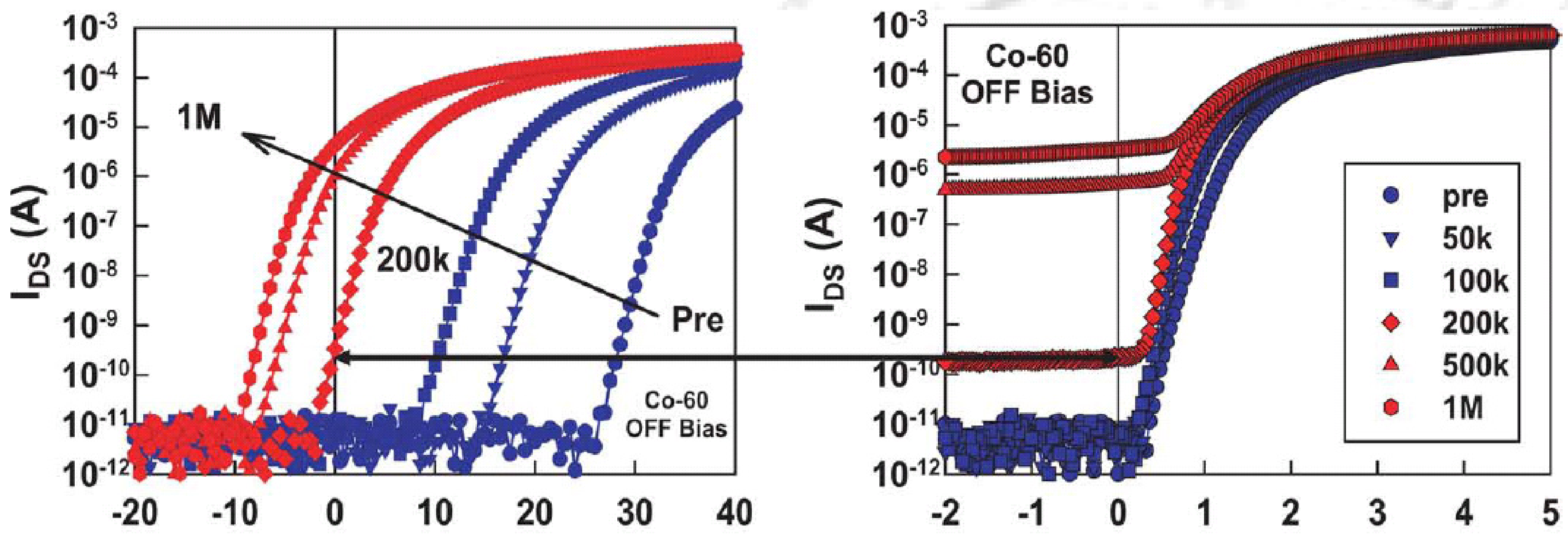
S. K. Dixit, et al., IEEE Trans. Nucl. 2007

- Thicker oxides, a return to charge trapping?
- Significant number of **electron traps** in HfO_2 in addition to hole traps
- **Minimal** charge trapping for thin HfO_2 with buffer SiO_2 layer



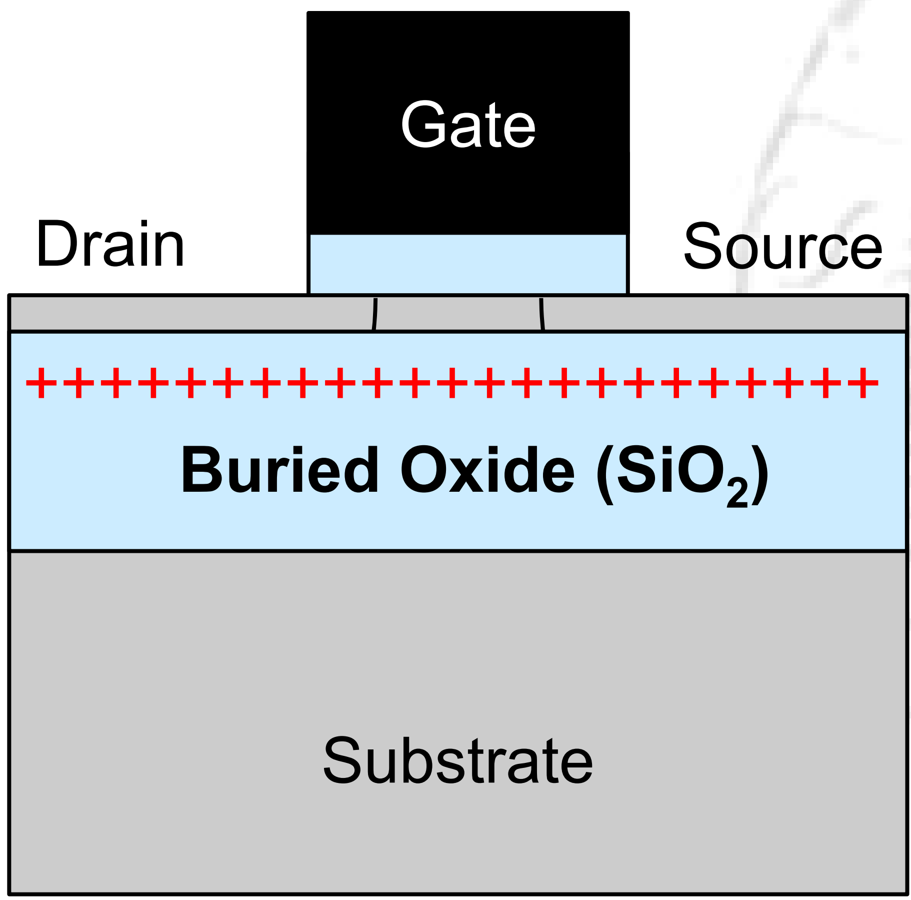
- Thick buried oxide sensitive to radiation
- Amount of charge trapping depends on SOI wafer technology (SIMOX vs wafer-bonding)
- **Parasitic Source-Drain leakage** develops in partially depleted devices

SOI: Partially Depleted Devices (2)

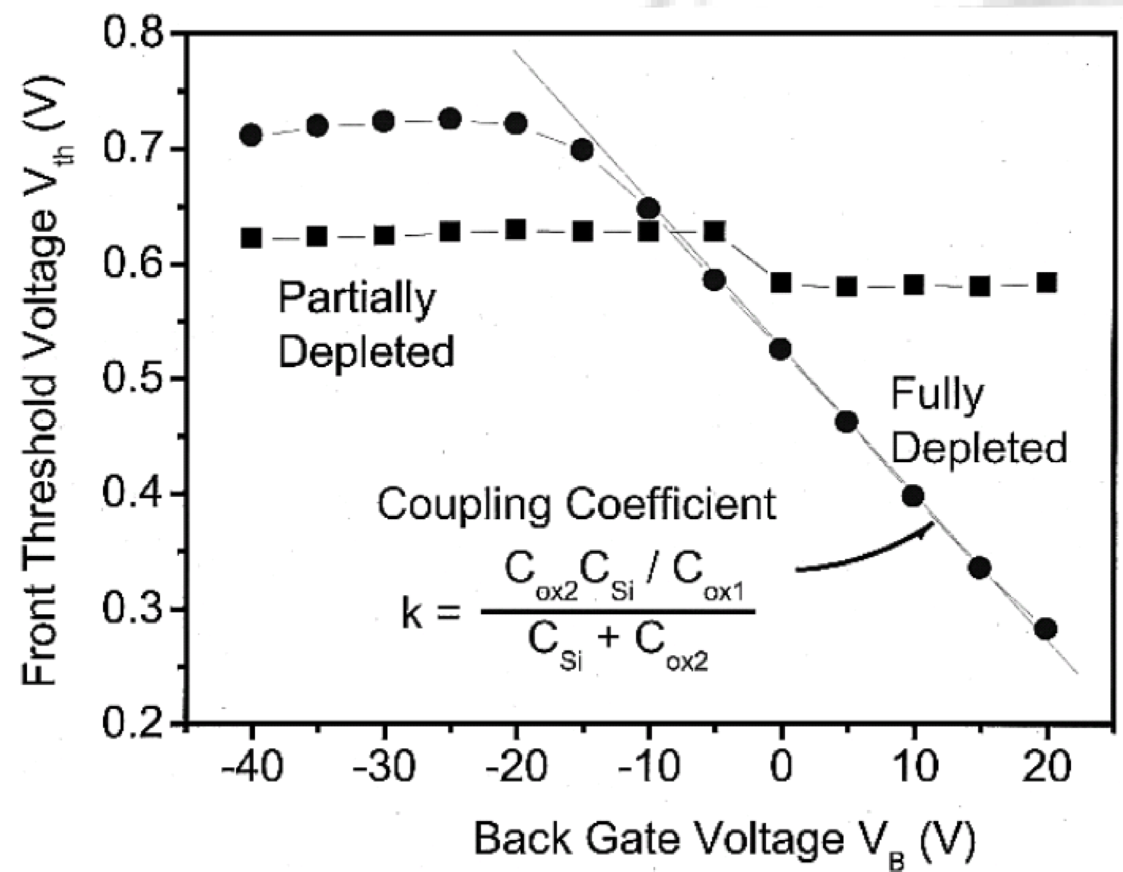


J.R. Schwank, et al., IEEE Trans. Nucl. 2008

- Threshold voltage shift in the parasitic back gate transistor leads to drain-source leakage



- Thick buried oxide sensitive to radiation
- Amount of charge trapping depends on SOI wafer technology (SIMOX vs wafer-bonding)
- Coupling with the back gate leads to **changes in the front gate transistor**



J.R. Schwank, et al., IEEE Trans. Nucl. 2003

- Coupling means back gate V_{th} shift leads to changes in front-gate V_{th}

- Stochastic effects due to a single particle hitting the sensitive area of a device
- SRAM
  - Single Event Upsets (SEU)
  - Single Bit Upsets (SBU)
  - Multiple Cell Upsets (MCU)
  - Muliple Bit Upsets (MBU)
- Combinational Logic
  - Single Event Transients (SET)

Simulated heavy ion e-h track in Si

DEDHIS Fer 275MeV

Log(e-h/cm3)

Profondeur (µm)

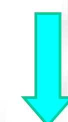
r (µm)

Electron-Hole density (cm^{-3})

Fe ions 275 MeV
LET=24 $MeVcm^2/mg$

LET metrics in Si:

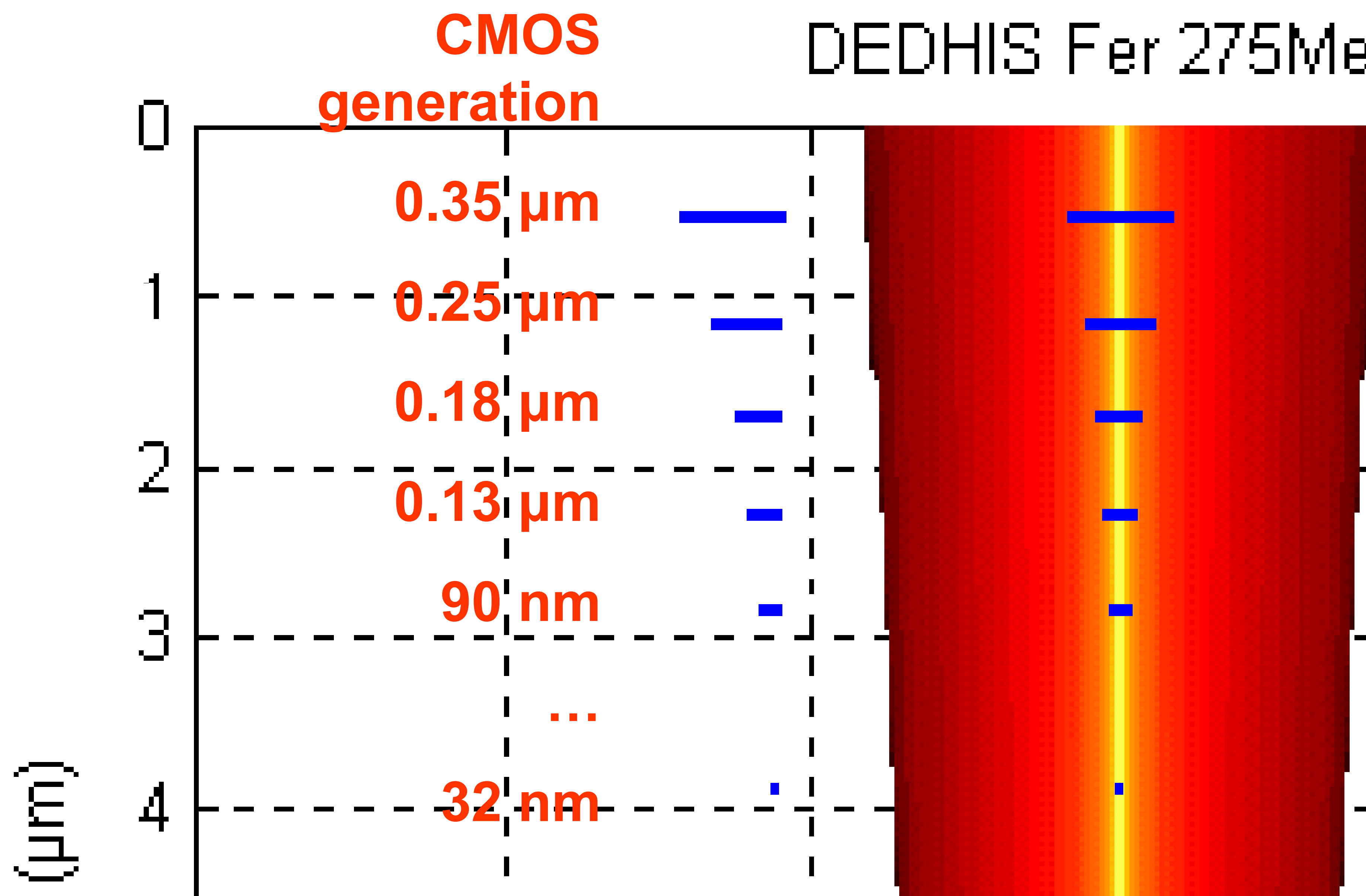
1 $MeVcm^2/mg$

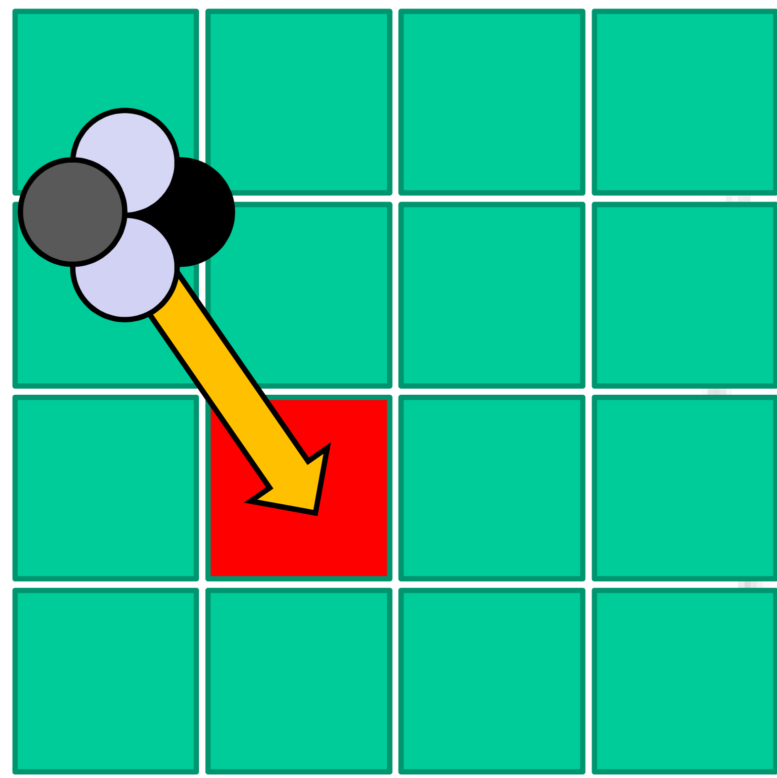


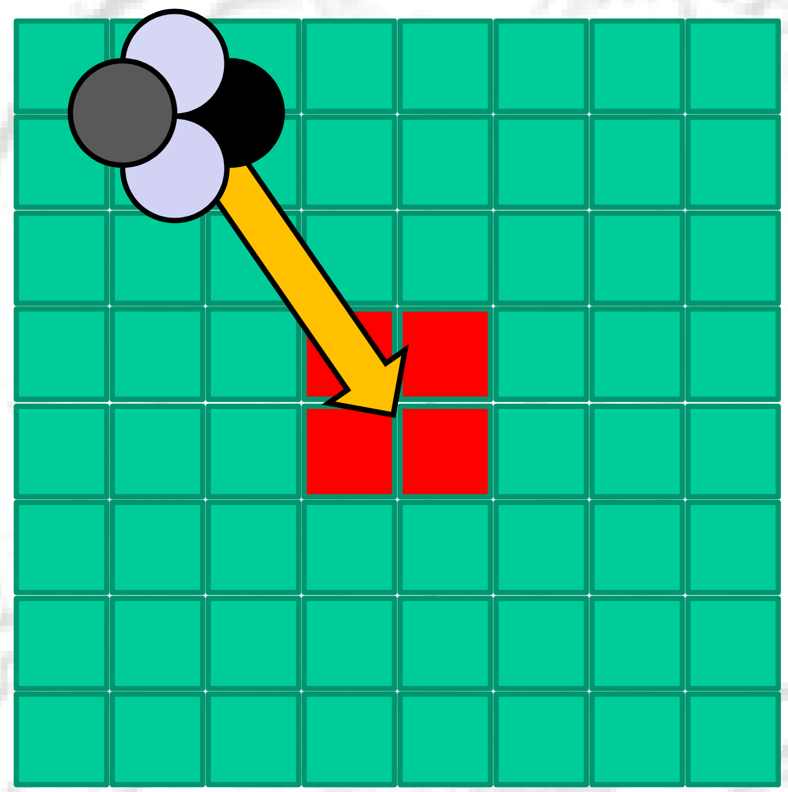
$6.4 \cdot 10^4$ e-h pairs/µm

10 fC/µm

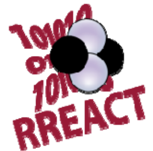
P. Foulliat, EWRHE 2004


CMOS generation
DEDHIS Fer 275Me
0
1
2
3
4
(µm)
0.35 µm
0.25 µm
0.18 µm
0.13 µm
90 nm
...
32 nm



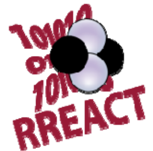


- Two generations after…



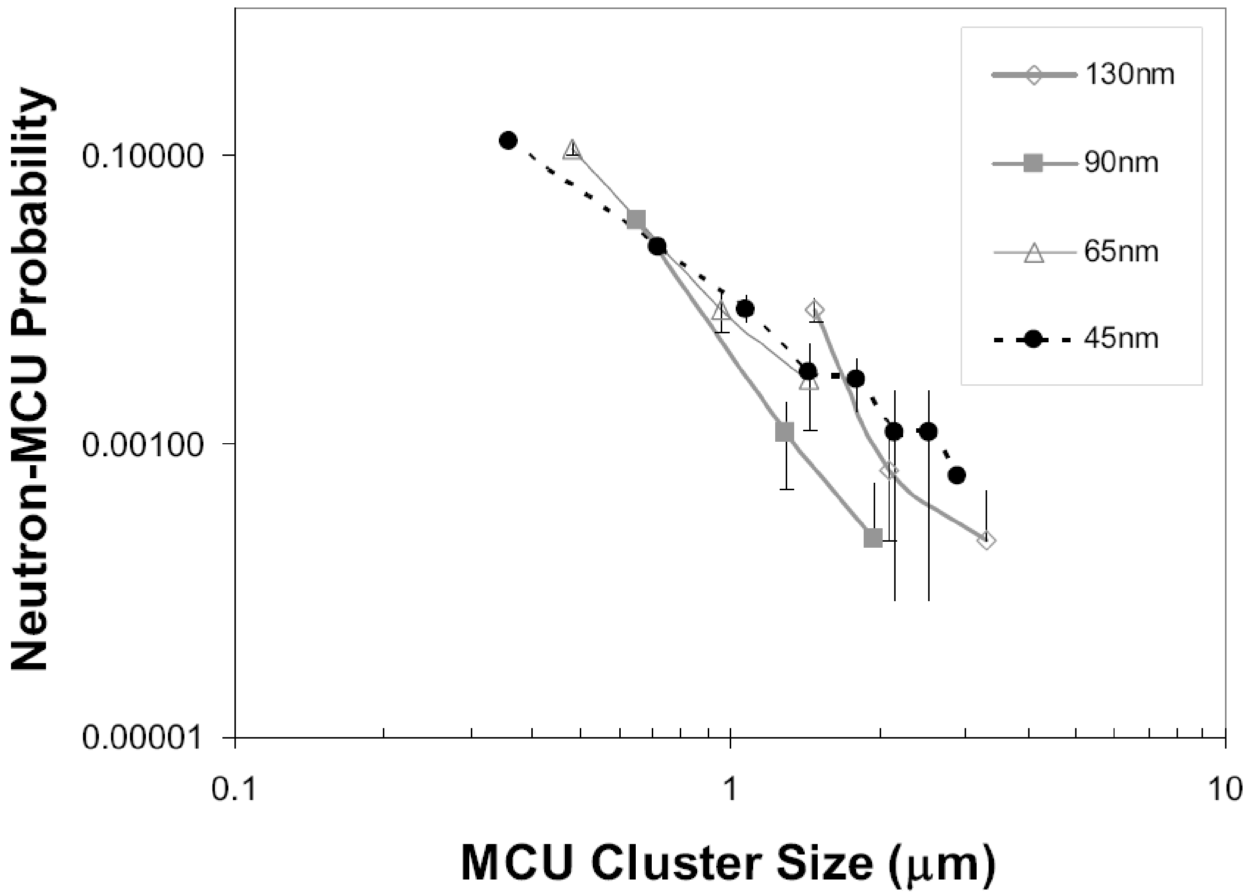
N. Seifert, et al., IRPS 2008

- SEU/bit constant or even decreasing!
- Area effect wins over reduction in capacitance



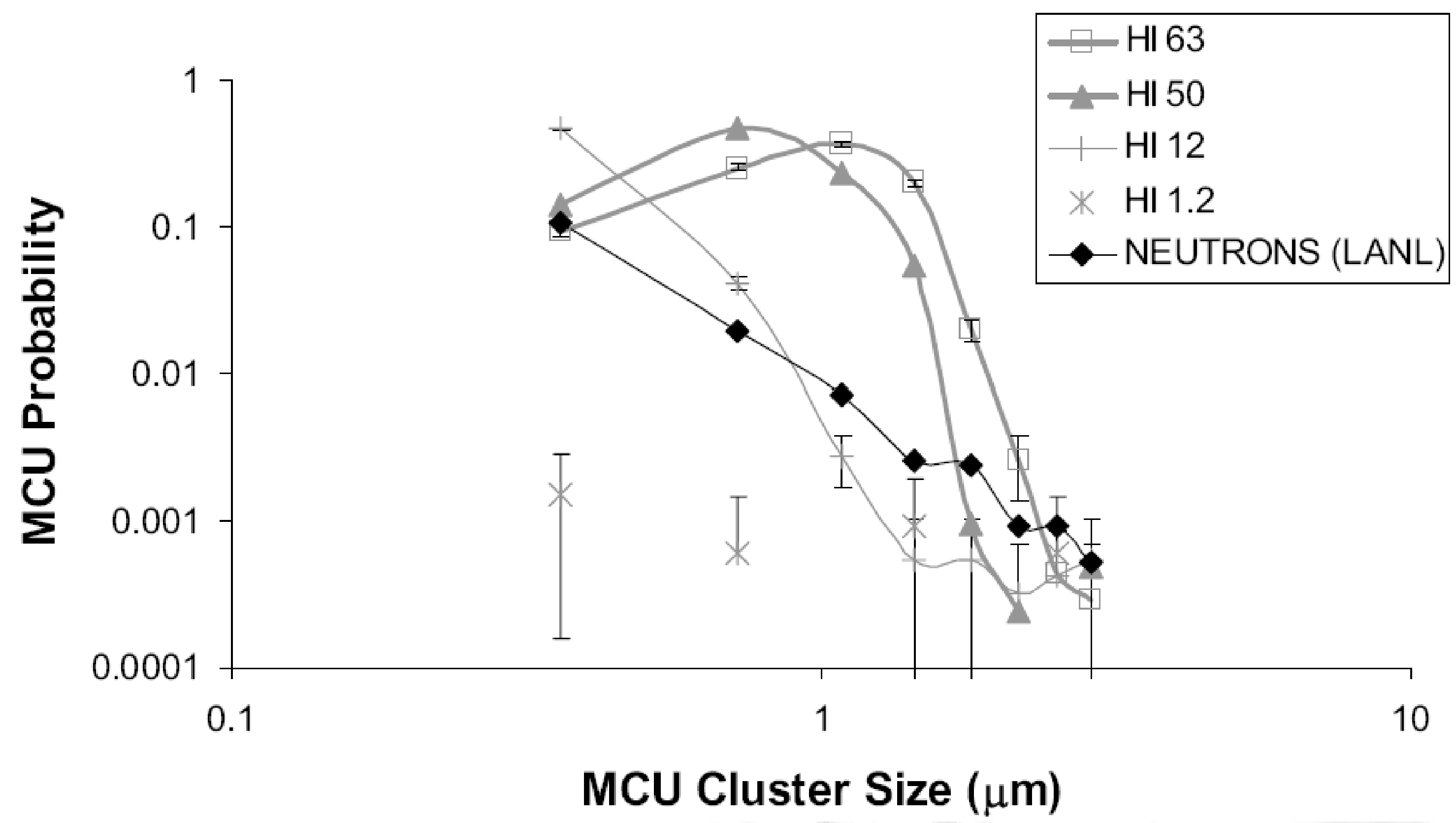
N. Seifert, et al., IRPS 2008

- Percentage of Multiple Bit Upsets increases (even more for other vendors)



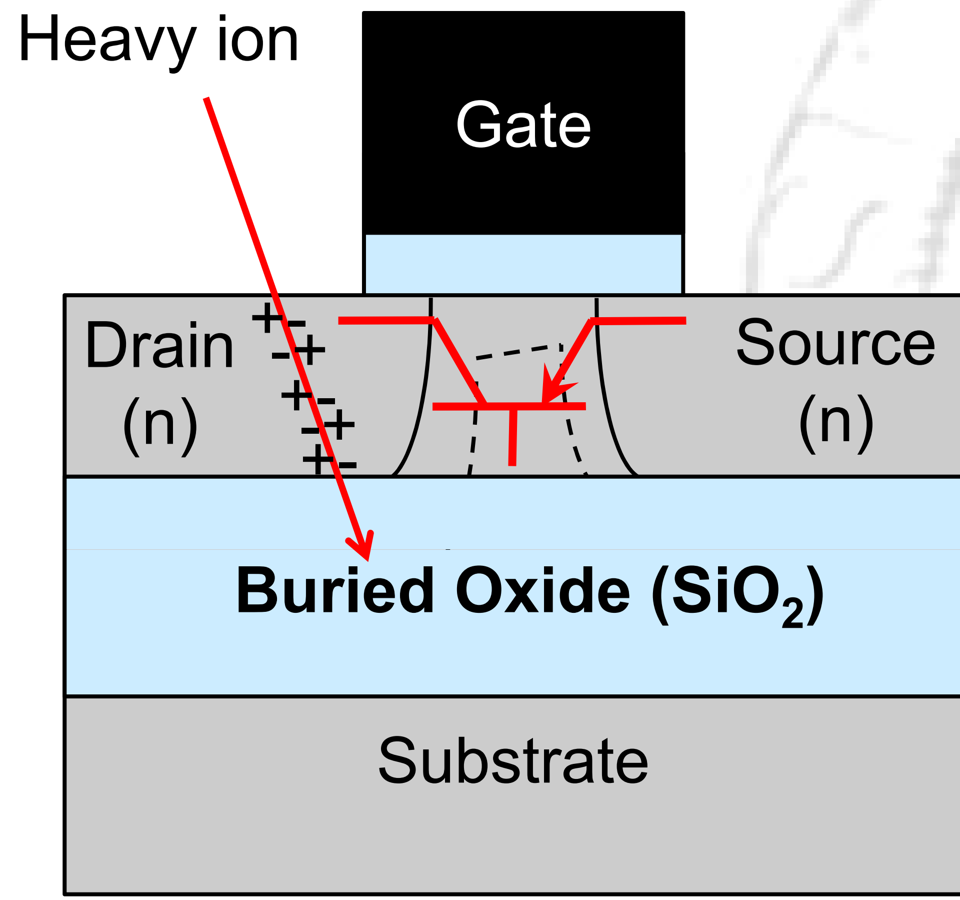
N. Seifert, et al., IRPS 2008

- MCU cluster size almost independent of technology node
- The number of affected bits grows with each generation



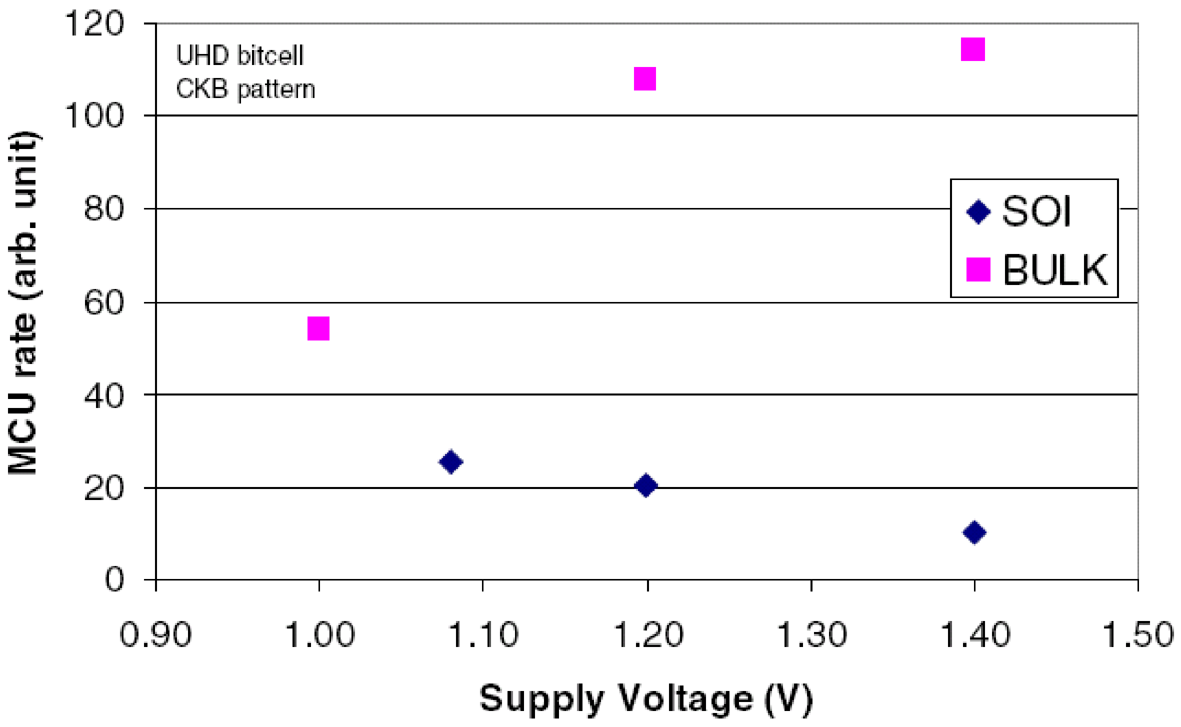
N. Seifert, et al., IRPS 2008

- Strong dependence on LET
- MCU's dominate at high LET



- Reduction of sensitive volume (less charge collection)
- Bipolar amplification may increase sensitivity
- Bipolar amplification important also on bulk devices

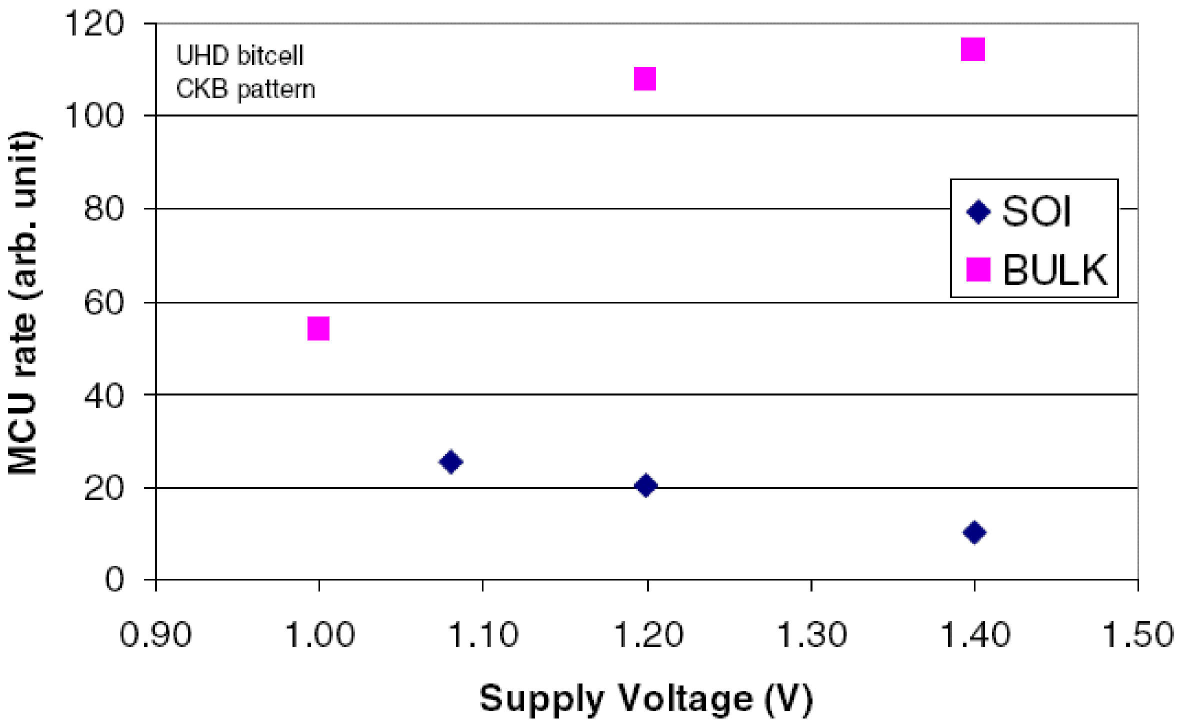
MCU: Bulk vs SOI



G. Gasiot, et al., IRPS 2008

- MCUs in some bulk technologies
  - occur preferentially along bitlines (inside p-wells)
  - increase with increasing supply voltage (contrary to SBU)
  - due to bipolar amplification ("battery" effect), increase in well potential due to particle strike affects many devices

MCU: Bulk vs SOI



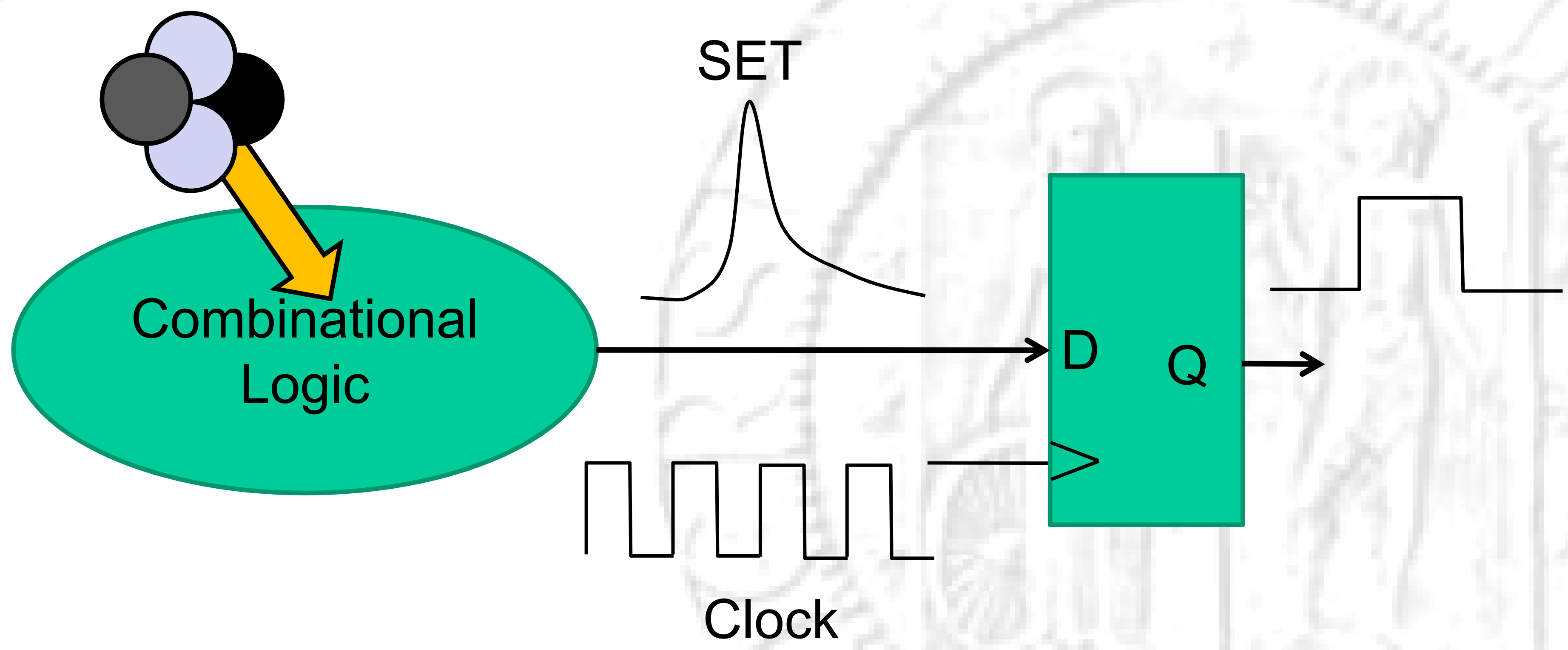
G. Gasiot, et al., IRPS 2008

- MCUs in SOI
  - due to geometrical effects
  - devices are separate (no common well)

- Memory elements aren’t the only resource sensitive to ionizing radiation, also **combinatorial logic** can be affected

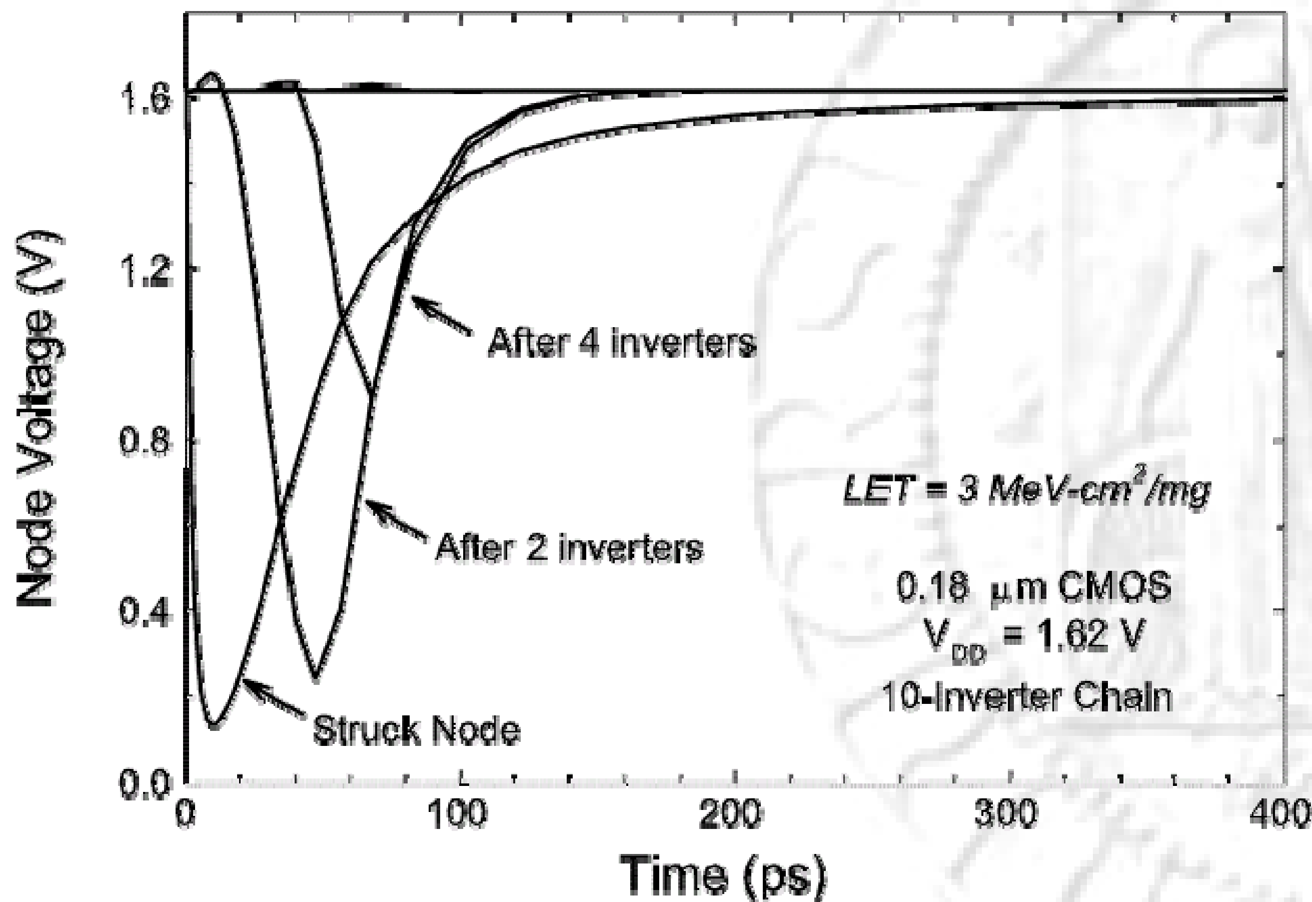
- Single Event Transients (SET) can originate from particle strikes in **reverse-biased pn junctions** belonging to the combinatorial part of a circuit

- SETs can eventually **propagate** to memory elements and be **latched**



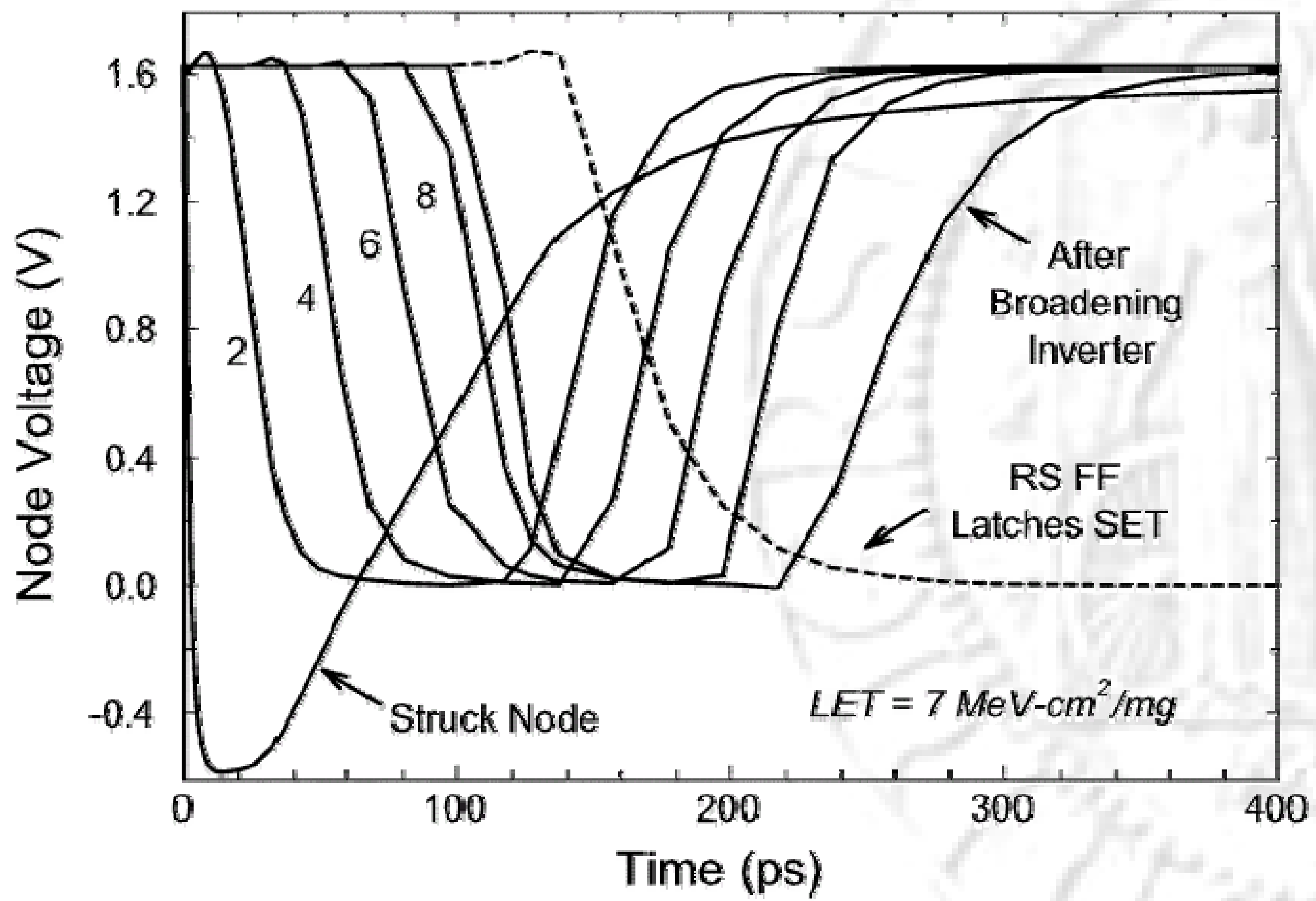
- **Logical** masking can block SET's
- The higher the frequency, the larger the probability of catching a transient (**temporal** masking)
- **Electrical** masking…

SET: attenuated propagation



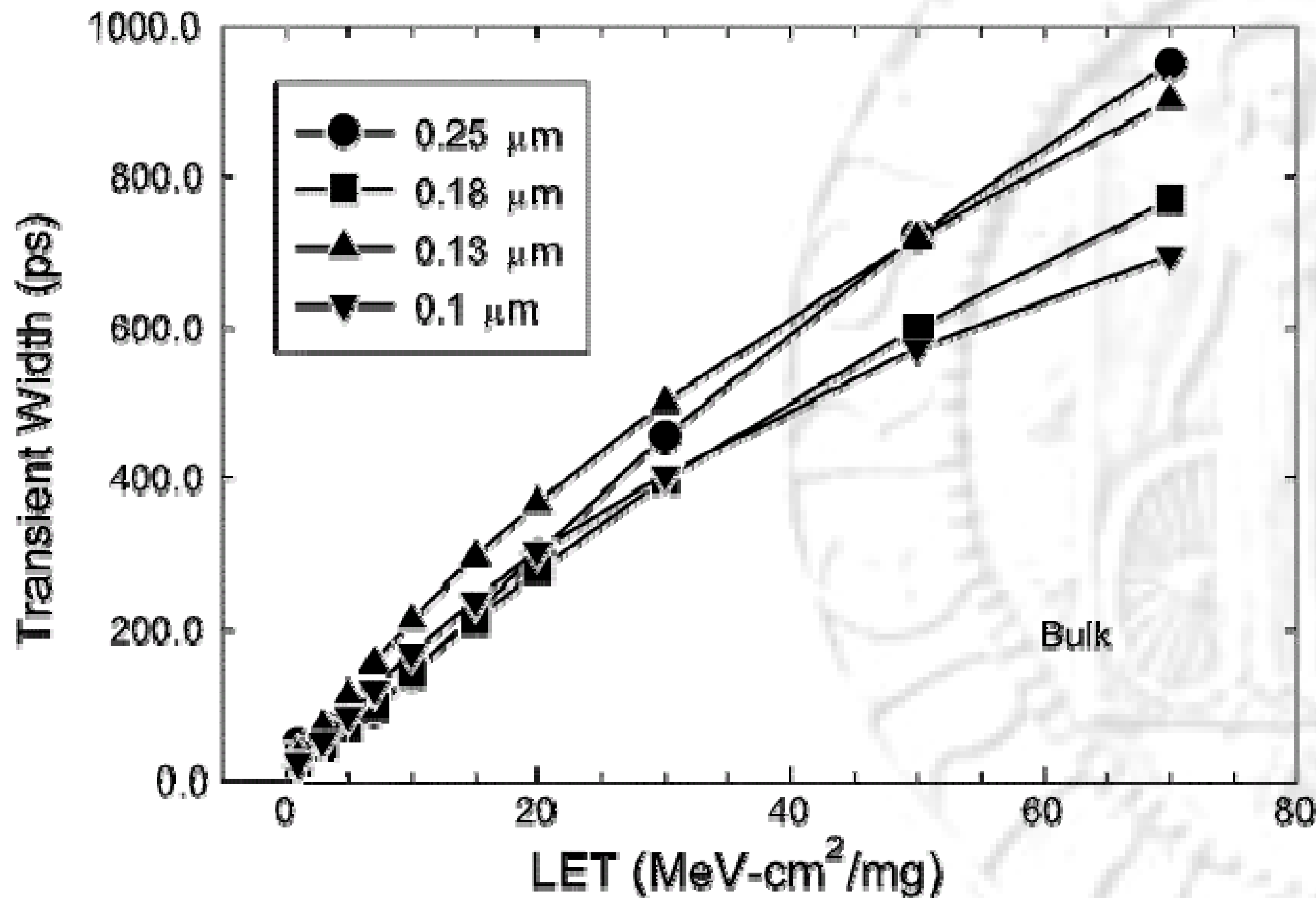
- Low LET below critical LET, attenuated propagation

P. Dodd et al., IEEE-TNS 2004



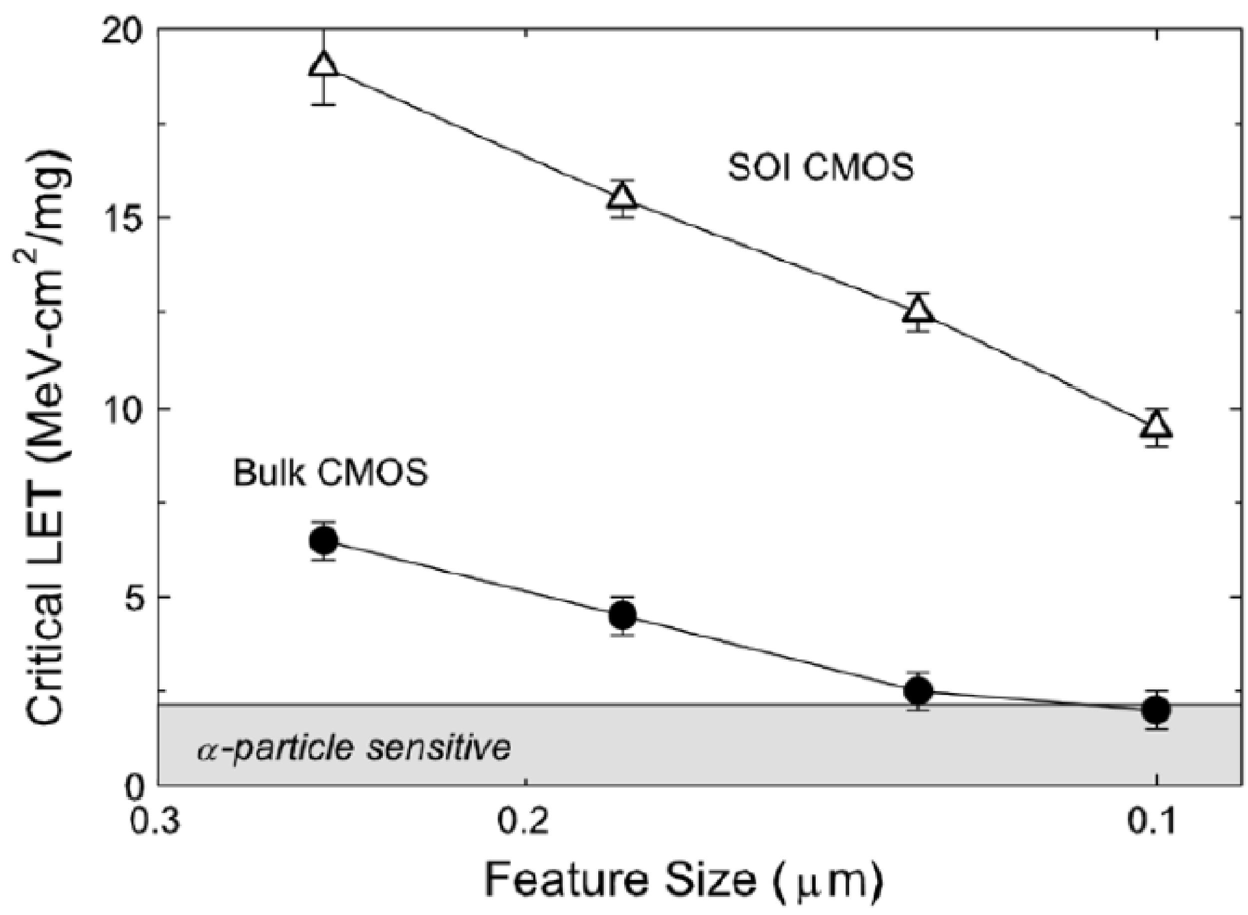
- High LET above critical LET, non-attenuated propagation

P. Dodd et al., IEEE-TNS 2004



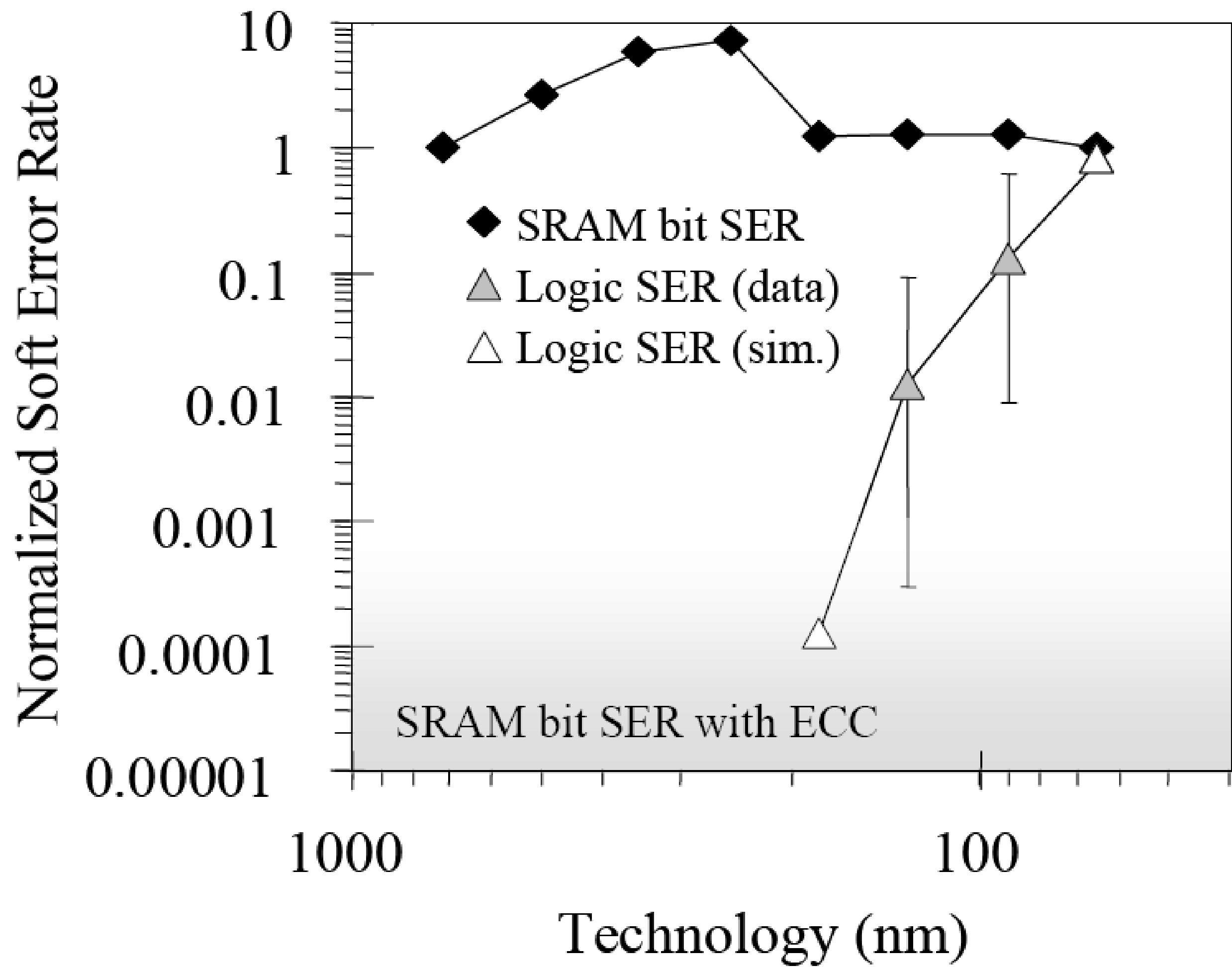
P. Dodd et al., IEEE-TNS 2004

- The higher the LET, the longer the pulse
- Complex dependence on technology



P. Dodd et al., IEEE-TNS 2004

- Critical LET for non-attenuated propagation decreases with feature size
- **SOI less sensitive** than bulk CMOS (shorter transients)



R. Baumann, IEEE-TDMR 2003

- SETs are expected to **dominate** the radiation sensitivity in future technologies, for high performance applications

- Simple scaling is no longer enough to sustain the pace of Moore's law, **new materials and device architectures** have been/will have to be introduced that may affect radiation response
- **Gate oxide sensitivity** to TID Effects has **improved** thanks to scaling, with no major issue from high-k layers. Isolation oxide may be still a problem
- **Radiation Induced Leakage Current** can be an issue for the reliability of Flash Memories and DRAMs
- The presence of the **buried oxide** in SOI may be detrimental to TID sensitivity but help with SEE
- **Multiple Cell/Bit Upsets** and **Single Event Transients** are a growing concern for digital circuits

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- All the referenced authors

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